USER'S REFERENCE MANUAL

GPIO-104

General Purpose Analog and Digital I/O for PC/104 Bus

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Conventions and Terminology used in this publication

Safety and Usage Conventions

Note:

Provides important information and useful tips that will assist in the understanding and operation of this product.

Caution:

Calls attention to a procedure, practice, or condition that could possibly cause equipment damage or bodily injury.

Danger:

Calls attention to a procedure, practice, or condition that is likely to cause extensive equipment damage, severe bodily injury, or death if not observed.

Terminology

Logic Conditions

Unless otherwise noted, logic signals are designated as TRUE (Set) and FALSE (Clear). Names with an asterisk (*) postscript are inverted or active low. Unless otherwise noted TRUE is considered logic '1' (+5Vdc or +3.3Vdc) and FALSE is considered logic '0' (0Vdc).

Numbering Systems

Computerized equipment often requires its numeric data to be represented in different forms depending on the audience and information being conveyed. Decimal numbers are typically used for end-user data entry and display while internally these values are converted and manipulated in native binary. Hexadecimal numbers are often used by programmers as an intermediate level between binary and decimal notations.

Base	Name	Format (MS ←→ LS)
2	Binary	0b10111001 or $1011\ 1001_2$
10	Decimal	185
16	Hexadecimal	0xB9 or $B9_{16}$ or HB9

Multi-Byte Word Formats

Unless otherwise specified numbers or registers spanning multiple bytes are stored in “little endian” format. The first address (ADDR+0) will contain the Least Significant Byte (LSB) while the Most Significant Byte (MSB) will reside at the highest address.

ADDR+0	ADDR	ADDR+n
LSB	LS ←→ MS	MSB

Introduction

The GPIO-104 is an 8-bit PC/104 compliant module designed to satisfy common analog and digital input/output requirements in a broad range of embedded applications. In many instances, the GPIO-104 will be the only peripheral module required. Standard functions include eight 12-bit multi-range analog inputs, four 12-bit multi-range analog outputs and 24 digital I/O channels.

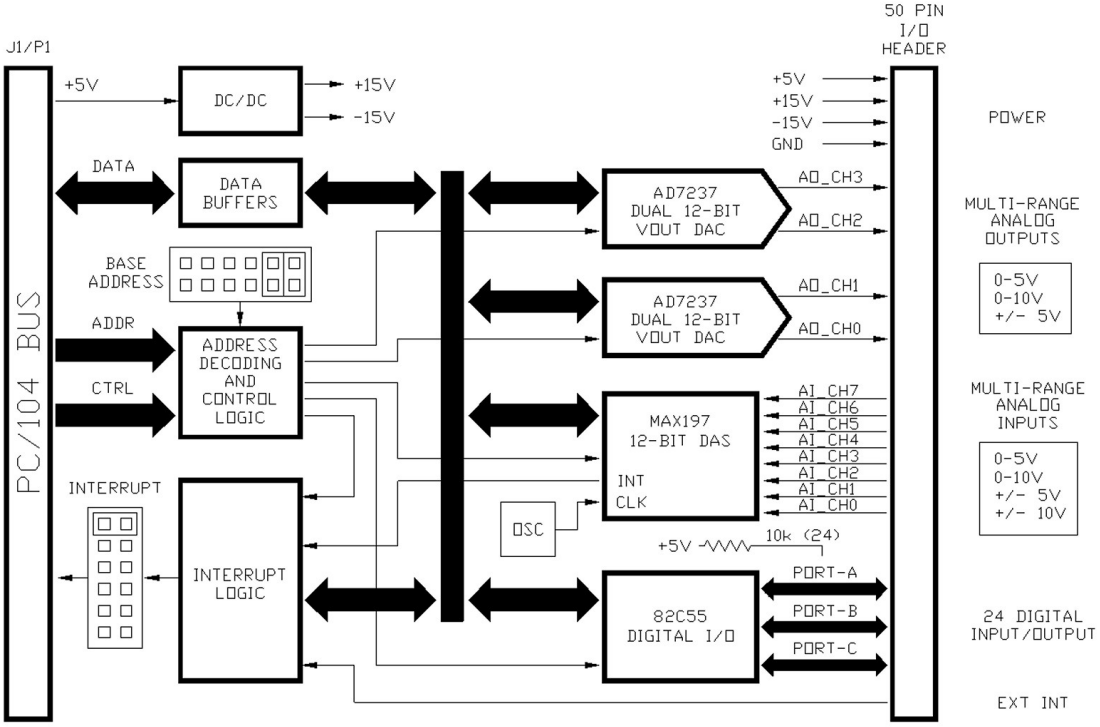


Figure 1 – GPIO-104 Simplified Block Diagram

Component Identification

To properly apply the GPIO-104 it is necessary to become familiar with its various components. The following figure and accompanying table briefly describe their functions and locations. Subsequent sections of this manual explain their purpose and configurations in greater detail.

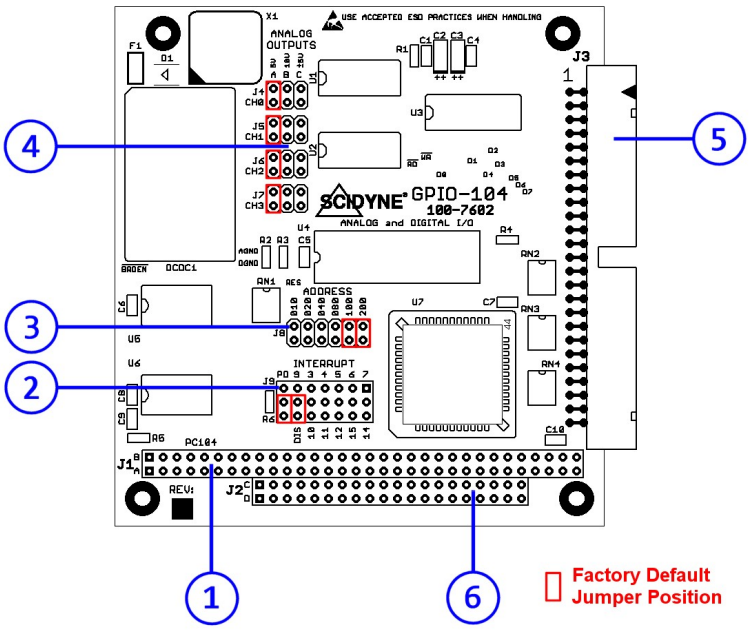


Figure 2 – GPIO-104 Component Identification

1 **PC/104 J1/P1 Connector**
This connector is the 8-bit PC/104 bus.

2 **Interrupt configuration jumpers (J9)**
This jumper block enables and sets which interrupt request line will be used by the GPIO-104 to interrupt the host. The optional J2/P2 connector must be installed if upper interrupt request lines (IRQ10, 11, 12, 14 or 15) will be used.

3 **Base Address Jumpers (J8)**
This jumper block determines the base address where the GPIO-104 will reside in the host's I/O map.

4 **Analog Output Range Jumpers (J4, J5, J6, J7)**
These jumper blocks configure the full-scale output range for each of the four analog outputs.

5 **I/O connector (J3)**
This 50-pin IDC header is used to connect the GPIO-104 to external devices. Please refer to Appendix-A for wiring information.

6 **Optional PC/104 J2/P2 Connector**
An optional 20-pin connector (J2/P2) can be installed to upgrade the GPIO-104 for 16 bit stack-through compatibility and to gain access to upper interrupt request lines.

Module Base Address and Register Map

Setting the Module Base Address

The GPIO-104 occupies 16 consecutive I/O bytes which can be set to begin on any 16-byte boundary within the host's I/O map. The factory default I/O address of 0x300 (768_{10}) is easily changed to accommodate any special requirements. The six position jumper block, J8, determines the base address. Each jumper position corresponds to a "weighted" I/O address as shown in the following table. The actual starting I/O address where the module resides is calculated by simply adding together the "weight" for each jumper that is installed. The values printed on the circuit board are in hexadecimal notation.

Addresses between 0x000 through 0x0ff are generally used by the host and should be avoided. Make sure the I/O address selected will not conflict with any other I/O hardware.

Example:

The factory default address is set by placing jumpers in positions 0x100 and 0x200.

Installed jumper	Address value "weight"
J8-5	0x100
J8-6	+ 0x200

	$0x300_{16}$ = 768_{10} = BASE ADDRESS

J8 Base Address Jumper Settings						
J8	-1	-2	-3	-4	-5	-6
Weight (Dec)	0x010 (16)	0x020 (32)	0x040 (64)	0x080 (128)	0x100 (256)	0x200 (512)
					Factory Default jumper positions	

Register Map

The various GPIO-104 peripheral devices are accessed at specific offsets relative to the base address. The following table illustrates their locations. Some of the locations are write-only, read-only or may be both written and read. Performing a read operation from a write-only location will return an indeterminate value. Writing to a read-only location will not cause a fault but should be avoided for reasons of future compatibility. Additionally, certain registers use only a few of the available data bits. When working with those registers, it is good practice to use software bit preservation techniques (AND, OR, bit-fields) so that only the meaningful bits will be examined and manipulated.

GPIO-104 I/O Register Summary

Byte Offset (dec)	Name	R/W	Host Data Bus							
			D7	D6	D5	D4	D3	D2	D1	D0
0	INTR_STATUS	R	X	X	X	X	X	X	EXT	DAS
1	AO_UPDATE	W	X	X	X	X	X	X	X	X
2	DAS_CTRL	W	PD1	PD0	ACQMOD	RNG	BIP	A2	A1	A0
	DAS_LB	R	B7	B6	B5	B4	B3	B2	B1	B0
3	DAS_HB	R	These bits read 0 in Unipolar mode (BIP = 0). In Bipolar mode (BIP = 1) these bits sign-extend the value of bit 11				B11	B10	B9	B8
4	AOCH0_LB	W	B7	B6	B5	B4	B3	B2	B1	B0
5	AOCH0_HB	W	0	0	0	0	B11	B10	B9	B8
6	AOCH1_LB	W	B7	B6	B5	B4	B3	B2	B1	B0
7	AOCH1_HB	W	0	0	0	0	B11	B10	B9	B8
8	AOCH2_LB	W	B7	B6	B5	B4	B3	B2	B1	B0
9	AOCH2_HB	W	0	0	0	0	B11	B10	B9	B8
10	AOCH3_LB	W	B7	B6	B5	B4	B3	B2	B1	B0
11	AOCH3_HB	W	0	0	0	0	B11	B10	B9	B8
12	PORTA	R/W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
13	PORTB	R/W	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
14	PORTC	R/W	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
15	DIO_CTRL	R/W	MODE SET FLAG	GROUP A				GROUP B		
				MODE		PA DIR	PC (HI)	MODE	PB DIR	PC (LOW)

Notes:

1) X = Not used or not implemented.

Analog Input / Output

The GPIO-104 provides eight 12-bit, single-ended, multi-range analog input channels and four 12-bit multi-range analog output channels. All analog signals are non-isolated and share the same GND potential as the host computer. The analog I/O signals are routed to connections on the 50-position IDC header, J3. Please refer to Appendix-A to determine signal locations.

Analog Inputs

A Maxim MAX197 chip is used to implement the eight analog inputs. This device is a complete multi-range DAS (Data-Acquisition-System) featuring software programmable parameters. Each channel can be individually configured to operate in one of four full-scale input ranges: ±10V, ±5V, 10V or 5V. This effectively increases dynamic range to 14-bits and provides the flexibility to interface 4-20ma and bipolar sensors. In addition, acquisition can be done automatically by the GPIO-104 hardware or under full control of the user's software. Optionally, the MAX197 can interrupt the host at the end of each conversion. The inputs channels are overvoltage protected to ±16.5V. This protection is active even when the GPIO-104 is not powered. An overvoltage condition on one or more channels does not affect the reading taken on the remaining channels.

To achieve the greatest performance, the analog inputs should be driven from low impedance sources, ideally OP AMPS with a settling time of 1.5µs or less. Attention must also be given to maintain signal integrity by using proper shielding, wiring, and grounding techniques.

DAS Control Register

base + 0x0002

Each analog-to-digital conversion process is started by writing to the **DAS_CTRL** register. This register is **write-only** and selects the analog input channel to be digitized, its range, conversion mode, and the type of acquisition (Internal or External) to be performed. Writing to this register also clears the **DAS** flag within the **INTR_STATUS** register. Reading from this location returns the most recent conversion lower-byte data.

Bit	7	6	5	4	3	2	1	0	
base + 0x0002	**PD1 = 0**	**PD0 = 0**	**ACQMOD**	**RNG**	**BIP**	**A2**	**A1**	**A0**	**DAS_CTRL**
Write only	W	W	W	W	W	W	W	W	
Reset	0	0	0	0	0	0	0	0	

PD1, PD0 **Clock Source and Power-Down modes**
For correct operation set Bit7 = 0 and Bit6 = 0, for External Clock

ACQMOD **Acquisition Mode**
0 = Internally controlled acquisition. 1 = Externally controlled acquisition

RNG **Range**
Selects the full-scale voltage at the input, 0 = 5V 1 = 10V

BIP **Conversion mode**
0 = Unipolar 1 = Bipolar

A2, A1, A0 **Input Channel Address**
These three bits determine which analog input channel the acquisition will be performed on.
A0 = LSB

Internal Acquisition

Internal acquisition is the simplest mode to implement and is frequently how the GPIO-104 is used. Select this mode by writing the **DAS_CTRL** register with the **ACQMOD** = 0. The desired input channel and range selection bits must also be written at this time. The write operation initiates an acquisition interval whose duration is internally timed and lasts approximately 3µs. Conversion automatically begins at the end of the acquisition interval and lasts an additional 6µs. The overall start-to-finish digitization process takes approximately 9µs.

External Acquisition

Use external acquisition for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write operations. The first operation, written with **ACQMOD** = 1, starts an acquisition interval of indeterminate length. The desired input channel and range selection bits are also written at this time. The second write operation, written with **ACQMOD** = 0, terminates acquisition and starts a conversion. However, if the second byte written contains **ACQMOD** = 1, another indefinite acquisition interval is started. The conversion time, once started, lasts approximately 6µs.

For external acquisition, the input channel and range selection bits must have the same values on the first and second write operations.

Reading a Conversion

After each conversion, the **DAS** flag within the **INTR_STATUS** register is set and generates an IRQ if interrupts are configured. The host can determine when a conversion is complete using three methods: by waiting longer than the overall acquisition and conversion time, by polling the **DAS** flag, or by having the **DAS** flag interrupt the host when it becomes set. The **DAS** flag is cleared on the first read operation or if a new **DAS_CTRL** control word is written. Another **DAS_CTRL** byte must be written to initiate another conversion.

Since the GPIO-104 uses an 8-bit bus interface, two I/O read operations are required to access the entire 12-bit value. The output data format is binary in unipolar mode with ***1LSB = (FS / 4096)*** and twos-complement binary in bipolar mode with ***1LSB = ((2 x |FS|) / 4096)***. The lower eight bits (B0-B7) reside at module offset 2. The four upper bits (B8-B11) are accessed at module offset 3 and appear on data bits D0-D3 respectively. The remaining four data bits (D4-D7) at offset 3 are either set low (in unipolar mode) or sign-extend the value of the MSB (bit-11) (in bipolar mode).

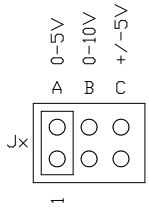
Analog Input Equations			
Input Range (Volts)	1_{LSB} (mv)	Vin Calculation	Value Calculation
0 to 5	1.2207mv	Vin = Value x 1.2207mv	Value = Vin / 1.2207mv
0 to 10	2.4414mv	Vin = Value x 2.4414mv	Value = Vin / 2.441mv
- 5 to + 5	2.4414mv	Vin = Value x 2.4414mv	Value = Vin / 2.4414mv
-10 to +10	4.8828mv	Vin = Value x 4.8828mv	Value = Vin / 4.8828mv

Analog Outputs

The four 12-bit analog outputs are produced by two AD7237 dual DAC (Digital-to-Analog Converter) chips. Each channel is jumper-selectable to operate in one of three popular full-scale output ranges, 10V, 5V or ±5V and are capable of driving ±5mA. A step-up DC/DC converter allows the 10V and bipolar ranges to be achieved while operating the GPIO-104 module from a single +5V supply. In addition, the DACs are double buffered. Data can be freely pre-loaded to any of the channels without immediately affecting their outputs. After each DAC to be changed is pre-loaded, writing any value to the **AO_UPDATE** register will cause those analog outputs to be updated simultaneously. The other DACs maintain their previous output voltages without interruptions or glitches. This feature is particularly useful when applying the GPIO-104 in "phase sensitive" applications.

Setting Output Range

Each channel's output range is independently set by a corresponding three-position jumper block as shown in the following table. The factory default setting is 0-5V (Position 'A').

Analog Output Configuration Jumpers		
Channel	Jumper Block	Full Scale Range
AOCH0	J4	
AOCH1	J5	
AOCH2	J6	
AOCH3	J7	

The following table shows the transfer equations for each range and resulting output voltages using various input values.

Analog Output Equations			
Value written to a DAC Channel	Output Range		
	0 - 5 Volts	0 - 10 Volts	±5 Volts
MSB LSB	1LSB = 1.2207mv Vo = 5 x (value/4096)	1LSB = 2.4414mv Vo = 10 x (value/4096)	1LSB = 2.4414mv Vo = (value/409.6) - 5
1111 1111 1111	+4.99878	+9.99756	+4.99756
1000 0000 0001	+2.50122	+5.00244	+0.00241
1000 0000 0000	+2.50000	+5.00000	0.00000
0111 1111 1111	+2.49878	+4.99756	-0.002441
0000 0000 0001	+0.00122	+0.00244	-4.99756
0000 0000 0000	0.00000	0.00000	-5.00000

Digital Input / Output

The GPIO-104 module uses an industry standard 82C55A Programmable Peripheral Interface chip to provide 24 non-isolated digital Input/Output channels across three 8-bit ports. This device is very versatile and offers flexible configuration, including software programable port directions and interrupt-driven strobed handshaking functions. Each channel features TTL/CMOS compatible signal levels and ±2.5mA drive capability. In addition, 10k pull-up resistors to +5V are provided on all 24 channels. This feature makes sensing open-collector, switches, and contact-closure type devices simple and straight-forward. All channels default to inputs during system reset. The reader should refer to the 82C55A manufacturer's data sheet for complete hardware and software details related to this device.

External components attach to the GPIO-104 through pins of connector J3, see Appendix-A. A companion terminal board (PN 100-7625/50) is available to make field wiring easier.

External Output Driver Circuits

Devices such as electro-mechanical relays generally operate at higher currents and/or voltages than can be supplied by GPIO-104 digital output. If additional drive capability is required, circuits like those shown can be used.

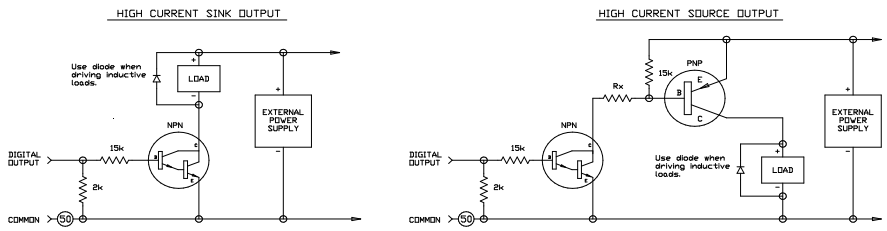


Figure 3 - External Output Driver Circuits

Over-Voltage Input Protection

The GPIO-104 digital inputs are designed to be compatible with and connect to other 5 Volt TTL/CMOS level signals. In some cases it may be necessary to connect to voltages much higher than the digital inputs could normally withstand. The best solution is to use a digital isolator or optical isolation, but this is not always practical or cost-effective. An inexpensive alternative is shown. Two switching diodes and a resistor form a simple input protection circuit. Both diodes are off whenever the input signal is within the normal TTL/CMOS range. Input signals above +5.6V will forward bias D1 and clamp the digital input to one diode drop above Vcc. If the input drops below ground by more than -0.6V then D2 conducts clamping the digital input to one diode drop below ground. In either condition the excess input voltage will appear across the resistor which limits the input current to a safe level. With the values shown, inputs of ±30V are easily handled. Each digital input driven by a high voltage must have its own protection circuitry.

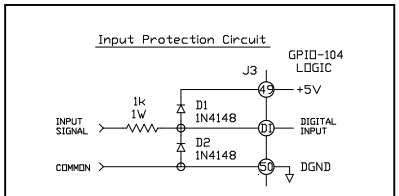


Figure 4 - Input Protection

Host Interrupts

The GPIO-104 can generate an interrupt to signal the completion of analog-to-digital conversions or to have external devices request special services from the host.

Host Interrupt Selection

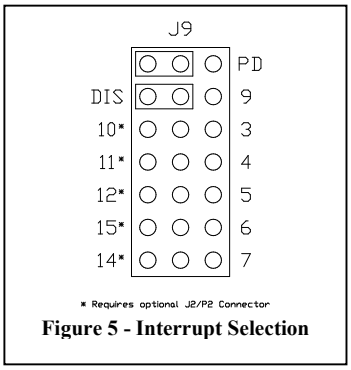


Figure 5 - Interrupt Selection

Jumper block J9 configures which host interrupt will be associated with the GPIO-104. All host interrupts are supported, but the optional J2/P2 connector is required to access the upper interrupt requests (IRQ10, 11, 12, 14, or 15). An interrupt is selected by placing a shorting jumper between the center row of J9 and the corresponding interrupt pin. Interrupt capability is disabled by placing a shorting jumper at the DIS position. The interrupt driver on the GPIO-104 conforms to the method for interrupt sharing as outlined in the PC/104 specification. This method recommends that one of the PC/104 modules sharing an IRQ provide a passive pull-down resistor to ground. The GPIO-104 can supply a 2K pull-down resistor when a shorting jumper is installed at the PD position of J9. The pull-down resistor has no effect when interrupts are disabled.

Try selecting an interrupt which is not currently being used by other system resources. Certain interrupts have a de facto standard usage and should be avoided. If interrupts must be shared, make sure all the software applications and hardware involved support interrupt sharing. To prevent excessive current draw and the possibility of erroneous operation, use only one pull-down per IRQ.

Interrupt Status Register

base + 0x0000

The Analog-to-Digital converter and external interrupt input share the same interrupt request to the host. When a GPIO-104 interrupt is generated, the host software can determine its source by examining the **INTR_STATUS** register. A bit set in either the **DAS** or **EXT** locations indicates the corresponding source requires service. The remaining six bits (B[7..2]) are not implemented and will return random information. The **INTR_STATUS** register functions even if interrupts are not used, allowing the host to utilize them for polling purposes.

Bit	7	6	5	4	3	2	1	0	
base + 0x0000	X	X	X	X	X	X	EXT	DAS	**INTR_STATUS**
Read only	R	R	R	R	R	R	R	R	
Reset	0	0	0	0	0	0	0	0	

EXT **External Interrupt**

A single, positive level-sensitive TTL compatible external interrupt is provided. An internal 2k pull-down resistor suppresses spurious interrupts when not used. The EXT bit of the **INTR_STATUS** register reflects the state of the **EXT_INT** input and generates a host IRQ while set. This signal is primarily intended to be used in conjunction with the digital I/O ports when implementing "Hand Shaking" functions.

DAS **Analog-to-Digital Converter**

The analog-to-digital converter sets the DAS flag after each conversion. The flag is cleared by reading the conversion result or by writing a new control word to the **DAS_CTRL** register.

Appendix - A J3, Input / Output Connections

Analog Ground	1▼	2	AICH7
Analog Ground	3	4	AICH6
Analog Ground	5	6	AICH5
Analog Ground	7	8	AICH4
Analog Ground	9	10	AICH3
Analog Ground	11	12	AICH2
Analog Ground	13	14	AICH1
Analog Ground	15	16	AICH0
AOCH3	17	18	AOCH2
AOCH1	19	20	AOCH0
Analog Ground	21	22	+15VDC Output [1]
-15VDC Output [1]	23	24	EXT_INT
PA7	25	26	PA6
PA5	27	28	PA4
PA3	29	30	PA2
PA1	31	32	PA0
PB7	33	34	PB6
PB5	35	36	PB4
PB3	37	38	PB2
PB1	39	40	PB0
PC7	41	42	PC6
PC5	43	44	PC4
PC3	45	46	PC2
PC1	47	48	PC0
+5VDC [2]	49	50	Digital Ground

Notes:

1) These supply outputs are provided to power external circuitry, ±10ma Max. They can withstand a momentary (1 Second) short circuit. Non-Isolated.

2) Supplied by Host. Non-Isolated and Unfused.

Appendix - B Specifications

Specification subject to change without notice

Analog Inputs:

General:	One MAX197 DAS chip provides eight multi-range single-ended analog input channels
A/D resolution:	12-bit (1 in 4096 of full-scale), 14-bit effective when using software range-switching techniques
Input ranges:	Each channel has software programmable input range: ±10V, ±5V, +5V or +10V
Input current:	Unipolar: 750µA max. Bipolar: 1200µA max.
Overvoltage:	±16.5V protection. A fault condition on any channel will not affect readings on other channels
Nonlinearity:	±1LSB
Sampling:	100, 000 samples/sec max. (Interrupt driven, host dependent), self-timed or user-controlled acquisition

Analog Outputs:

General:	Two AD7237 chips provide four multi-range analog output channels. Supports simultaneous updates
D/A resolution:	12-bit (1 in 4096 of full scale)
Output ranges:	Each channel has jumper selectable output range: ±5V, +5V or +10V
Output current:	±5mA max. per output
Settling time:	8µs max. to within ±½LSB of final value
Relative accuracy:	±1LSB
Nonlinearity:	Less than ±1LSB, guaranteed monotonic

Digital I/O:

General:	One 82C55A chip provides 24 digital I/O channels across three 8-Bit ports. Supports modes 0-2
Compatibility:	5V TTL/CMOS levels. Each channel is capable of ±2.5mA, 10k pull-up to +5V on each channel

Addressing: 8-bit PC/104 bus. Can be jumped for any 16 byte block in hosts I/O map, $0x000_{16}$ through $0x3f0_{16}$

Interrupt: One interrupt, jumper selectable IRQ 3, 4, 5, 6, 7, 9, (10, 11, 12, 14 or 15)*. Fully supports sharing. Used by Analog-to-Digital converter and positive-level-sensitive external interrupt.

Power: +5vdc ±5% @ 340mA typical, Unloaded outputs

Dimensions: PC/104 compatible, 3.55"W x 3.77"L x 0.8”H. 8-bit stack-through, optional 16-bit stack-through

Environmental:

Operation:	-25°C to 65°C (Standard) Non-condensing relative humidity: 5% to 95%
Compliance:	RoHS, Lead-Free

Product Origin: Designed, Engineered, and Assembled in U.S.A. by SCIDYNE® Corporation using domestic and foreign components.