USER'S REFERENCE MANUAL

RELAYIO-104

Relay Output / Isolated Input PC/104 Module

Model No.	100-7610		
Doc. No.	M7610	Rev: 1.5	3/15/21

SCIDYNE®

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Conventions and Terminology Used in this Publication

Safety and Usage Conventions

Note:

Provides important information and useful tips that will assist in the understanding and operation of this product.

Caution:

Calls attention to a procedure, practice, or condition that could possibly cause equipment damage or bodily injury.

Danger:

Calls attention to a procedure, practice, or condition that is likely to cause extensive equipment damage, severe bodily injury, or death if not observed.

Terminology

Logic Conditions

Unless otherwise noted, logic signals are designated as TRUE (i.e.; Set, logic '1', +5Vdc or +3.3Vdc) and FALSE (i.e.; Clear, logic '0', 0Vdc). Names with an asterisk (*) postscript are inverted or active low.

Numbering Systems

Computerized equipment often requires its numeric data to be represented in different forms depending on the audience and information being conveyed. Decimal numbers are typically used for end-user data entry and display while internally these values are converted and manipulated in native binary. Hexadecimal numbers are often used by programmers as an intermediate level between binary and decimal notations.

Base	Name	Format (MS ← -- →LS)
2	Binary	0b10111001 or $1011\ 1001_2$
10	Decimal	185
16	Hexadecimal	0xB9 or $B9_{16}$ or HB9

Multi-Byte Word Formats

Unless otherwise specified numbers or registers spanning multiple bytes are stored in “little endian” format. The first address (ADDR+0) will contain the Least Significant Byte (LSB) while the Most Significant Byte (MSB) will reside at the highest address.

ADDR+0	ADDR	ADDR+n
LSB	LS ← -- →MS	MSB

Introduction

The RELAYIO-104 features eight independent "dry-contact" relay outputs and eight independent optically isolated AC/DC digital inputs. It physically conforms to the PC/104 standard, uses a single 40-pin IDC type header for all external I/O connections and operates on a single +5Vdc power source. The printed circuitry and I/O circuitry has been engineered to provide a maximum 250V isolation between the PC/104 bus and externally connected devices.

The 250V isolation specification applies only to input-to-board or board-to-output potential and not the potential between individual I/O channels even though all I/O channels are isolated from each other. The maximum inter-channel potential is limited to 100V.

The eight relay outputs are SPDT (Form-C) "dry-contact" closures, each providing three independent connections; COMMON, NORMALLY OPEN and NORMALLY CLOSED. All relays are de-energized (Normally Closed) during power off and system reset.

Each of the eight digital inputs can accept either AC or DC voltages in the range of 3V to 24V. In addition, the channels have input filters which can be individually enabled to allow AC frequencies as low as 40hz to be sensed reliably. Input #0 can also serve as an interrupt to the PC/104 host computer.

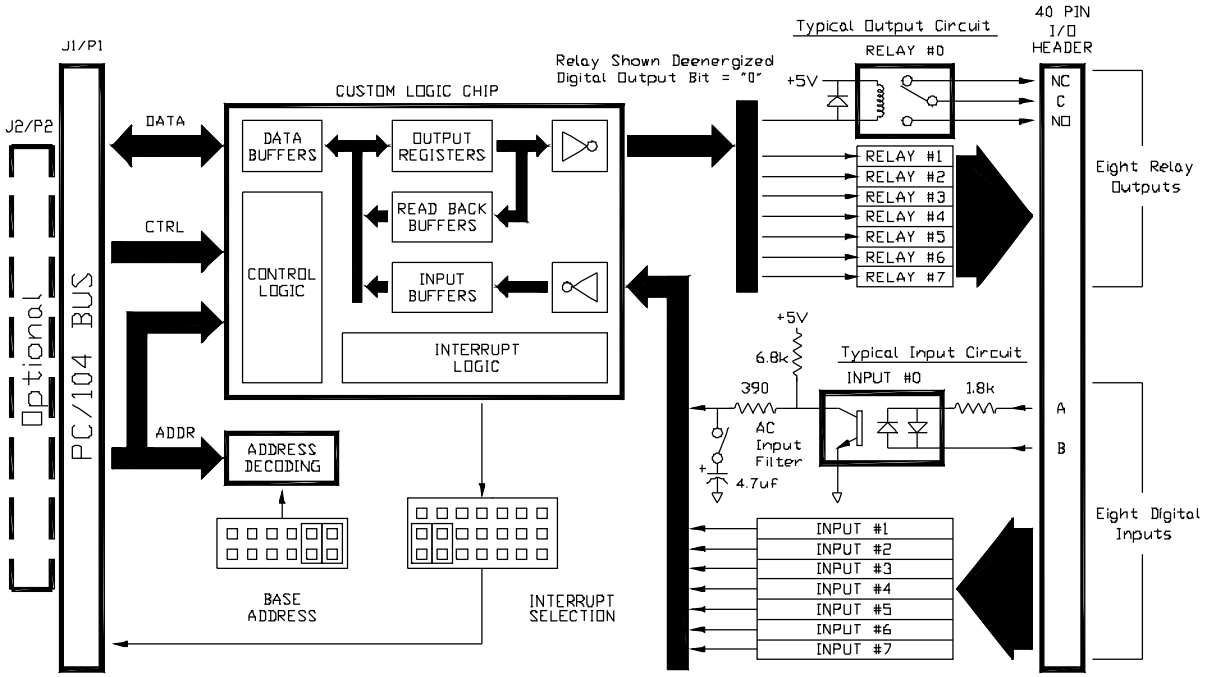

Figure 1 - RELAYIO-104 Simplified Block Diagram

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Component Identification

Before the RELAYIO-104 can be put into service it must be properly configured for the desired operating modes. This is accomplished by placing shorting jumpers and by setting switches located at various positions on the module. The component identification is shown in Figure 2.

Each RELAYIO-104 comes from the factory set to a basic functional default configuration. The user is free to change the default settings to satisfy any particular application requirements. A full explanation for each setting appears in subsequent sections of this manual.

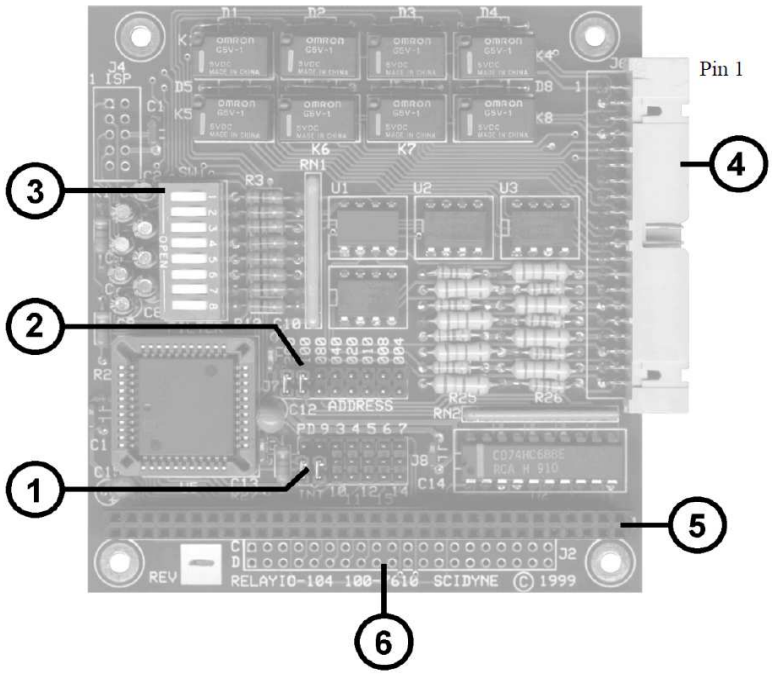


Figure 2 - Component Identification

(1) Interrupt Configuration Jumpers (J8)

This jumper block enables and sets which interrupt request line will be associated with the RELAYIO-104. The optional J2/P2 connector (Item 6) must be installed if upper interrupt request lines (IRQ10, 11, 12, 14 or 15) will be used.

(2) Base Address Jumpers (J7)

This jumper block determines the base address where the RELAYIO-104 will reside in the host's I/O map.

(3) AC Input Filter Switches

These eight switches correspond to the eight digital inputs. A switch in the "ON" or "CLOSED" position activates a low-pass filter for the respective digital input and enables reliable AC signal monitoring. Switch #1 corresponds to digital input #0 and so on.

(4) I/O Connector (J6)

This 40-pin IDC header is used to connect the RELAYIO-104 to external devices.

(5) PC/104 J1/P1 Connector

This connector is the 8-bit PC/104 bus.

(6) Optional PC/104 J2/P2 Connector

An optional 20-pin connector (J2/P2) can be installed to upgrade the RELAYIO-104 for 16-bit stack-through compatibility and to gain access to upper interrupt request lines.

Module Base Address and Register Map

Setting the Module Base Address

The RELAYIO-104 occupies 4 consecutive I/O bytes and can be placed on any 4 byte boundary within the host's I/O map. The factory default I/O address is 0x300 (768) but is easily changed to accommodate any special requirements. The eight position jumper block, J7, determines the base address. Each jumper position corresponds to a "weighted" I/O address as shown in the following table. The module's starting I/O address is calculated by simply adding together the "weight" for each jumper that is installed.

Addresses between 0x000 through 0x0ff are generally used by the host and should be avoided. Make sure the I/O address selected will not conflict with any existing I/O hardware.

J7 Base Address Jumper Settings								
J7	-1	-2	-3	-4	-5	-6	-7	-8
Weight (Dec)	0x200 (512)	0x100 (256)	0x080 (128)	0x040 (64)	0x020 (32)	0x010 (16)	0x008 (8)	0x004 (4)

Shaded area represents J7 factory default installed jumper positions. All other positions are left open. The values printed on the circuit board are in hexadecimal notation.

Example: The factory default address is set by placing jumpers at 0x100 and 0x200.

Installed jumper	Address Value "Weight"	
	Hexadecimal	Decimal
J7-2	0x100	256
J7-1	0x200	512
	---	---
Base Address:	0x300	768

Register Map

The various RELAYIO-104 peripheral functions are accessed at specific offsets relative to the base address. Some locations are write-only, read-only or may be both written and read. Performing a read operation from a write-only location will return an indeterminate value. Writing to a read-only location will not cause a fault but should be avoided for reasons of future compatibility.

Base Offset	Register Name	R/W	Host Data Bus							
			D7	D6	D5	D4	D3	D2	D1	D0
0	DOUT_REG	R/W	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
1	DIN_REG	R	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
2	INT_STAT	R	0	0	0	0	0	0	0	IS
		W	X	X	X	X	X	X	X	X
3	Reserved	NA	X	X	X	X	X	X	X	X

X = Not used, Not implemented, Undefined, or Don't care

Hardware and Software Details

General

External devices attach to the RELAYIO-104 through J6, a 40-pin IDC type connector. The pin-out for J6 is shown below.

Observe proper precautions when connecting to J6. Always remove power to the PC/104 computer and all external devices before connecting or disconnecting any attachments to J6. Before re-applying power, verify that all connections made to J6 are oriented correctly.

The J6 PIN #1 designation is printed on the circuit board and may also be identified by a small triangle ▼ molded into the connector's plastic shroud.

J6, Input / Output Header Connections

OUT7 COM	1▼	2	OUT7 NO
OUT7 NC	3	4	OUT6 NO
OUT6 NC	5	6	OUT6 COM
OUT5 COM	7	8	OUT5 NO
OUT5 NC	9	10	OUT4 NO
OUT4 NC	11	12	OUT4 COM
OUT3 COM	13	14	OUT3 NO
OUT3 NC	15	16	OUT2 NO
OUT2 NC	17	18	OUT2 COM
OUT1 COM	19	20	OUT1 NO
OUT1 NC	21	22	OUT0 NO
OUT0 NC	23	24	OUT0 COM
IN7 A	25	26	IN7 B
IN6 A	27	28	IN6 B
IN5 A	29	30	IN5 B
IN4 A	31	32	IN4 B
IN3 A	33	34	IN3 B
IN2 A	35	36	IN2 B
IN1 A	37	38	IN1 B
IN0/INT A	39	40	IN0/INT B

OUT = Relay Output, IN = Digital Input, INT = Interrupt Input
NC = Normally Closed, NO = Normally Open, COM = Relay Common

Relay Outputs

The RELAYIO-104 has eight independent sealed SPDT (form C) relay outputs. To ease wiring constraints and permit flexible mixing of AC and DC signals, the Normally-Closed (NC), Normally-Open (NO) and Common (COM) contacts from each relay are available separately on connector J6. The relays are capable of handling loads up to 1A @ 24Vdc or 0.5A @ 125VRMS. Break-Before-Make operation assures the Normally-Closed and Normally-Open contacts will never be mechanically connected to each other or to the relays COM contact at the same time.

Inductive loads often generate voltages with enough potential to cause arcing between a relay's contacts. This effect can cause problems in some situations and inevitably reduces the life-time of the contacts. When driving inductive loads it is suggested that an appropriate "Snubber" network be used across the contacts to dissipate any inductive spikes that may occur.

DOUT_REG - Digital Output Register 0x00

The relay outputs are controlled by the 8-bit register **DOUT_REG**. Each bit of this register corresponds to one of the eight relay outputs as shown.

Writing a bit as "0" causes the corresponding relay to turn off (COM connected to NC) while writing a "1" activates the relay (COM connects to NO).

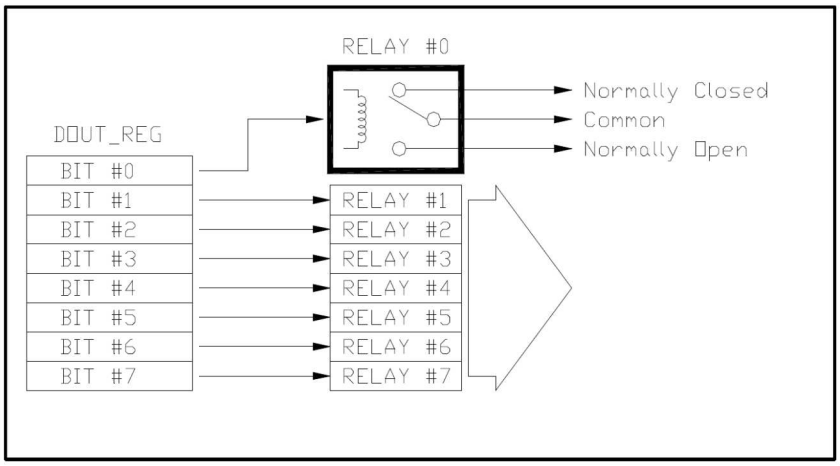


Figure 3 - DOUT_REG Functional Diagram

This register is both readable and writable allowing Read-Modify-Write bit manipulation software techniques to be used. The **DOUT_REG** is automatically cleared to all zeros during a system reset.

Bit	7	6	5	4	3	2	1	0	
(0x00)	**OUT7**	**OUT6**	**OUT5**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**	**DOUT_REG**
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

OUT[7:0] **Relay Output Control Bits**

These bits control and report the status of the relay outputs

Bit = 0: Corresponding relay de-activated, COM and NC contacts connected

Bit = 1: Corresponding relay activated, COM and NO contacts connected

Digital Inputs

The RELAYIO-104 has eight digital inputs. Each input uses a separate non-polarized optical coupler to provide electrical isolation between the host and the external AC/DC driving signal as well as isolation between the individual I/O channels.

Digital inputs can not be activated by simply connecting their associated “A” and “B” terminals together; i.e.: by means of a simple contact closure. The input circuitry requires an external power source with sufficient voltage and current to illuminate the optical coupler input LED.

Some devices such as PLCs (Programmable-Logic-Controllers) do not separate each of their outputs from each other. In these situations the RELAYIO-104's “A” signal inputs are often ganged together and connected to a power source at the PLC. The input-to-board isolation is still preserved but the digital inputs are now referenced to each other and share the same potential. This configuration can simplify and reduce wiring over long distances. An input is activated by pulling the corresponding “B” input to common, typically by means of an open-collector transistor output generated by the PLC.

DIN_REG - Digital Input Register 0x01

The status of the digital inputs is stored in a register called **DIN_REG**. The eight bits correspond to the eight digital inputs. When an input is energized the corresponding bit will be logic “1”. Likewise, a de-energized input will appear as logic "0”.

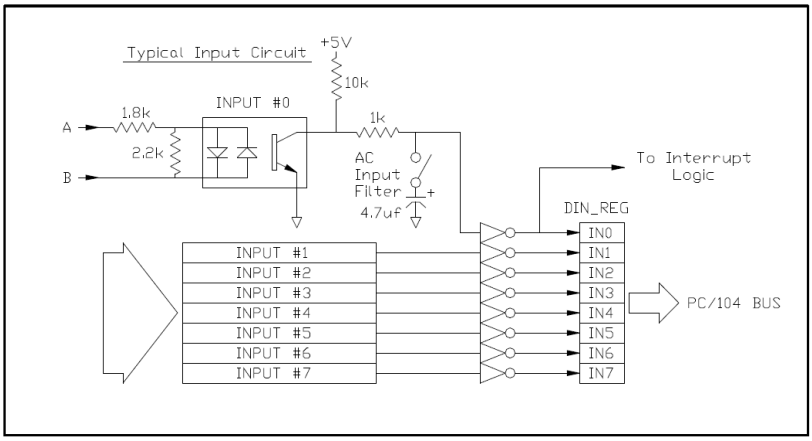


Figure 4 - DIN_REG Functional Diagram

Bit	7	6	5	4	3	2	1	0	
(0x01)	**IN7**	**IN6**	**IN5**	**IN4**	**IN3**	**IN2**	**IN1**	**IN0/INT**	**DIN_REG**
Read / Write	R	R	R	R	R	R	R	R	
Reset	X	X	X	X	X	X	X	X	

IN[7:0] **Digital Input Status Bits**

These bits represent the status of the digital inputs.
Bit = 0: Corresponding input de-activated
Bit = 1: Corresponding input activated

AC Input Filters

The optical isolators used in the digital input circuitry are designed to accept AC signals. However, the corresponding bits in the **DIN_REG** will momentarily switch between logic "1", "0" and back to "1" as the input signal crosses through zero volts while changing polarity. Depending on when the host application reads the **DIN_REG** the bits can be misinterpreted even though a steady state AC signal is applied. To overcome this condition the RELAYIO-104 is equipped with a low-pass filter on each of the inputs.

DIP switch SW1 is used to selectively enable the filter for each input. A switch in the "ON" or "CLOSED" position enables the filter for that particular digital input. The filters do not affect the input impedance of the digital inputs.

Inputs which are controlled by DC signals may also benefit by using the AC filters. If the input is being driven over a long distance or if the DC signal is excessively noisy enabling the filter can help minimize erroneous readings.

SW1 AC Input Filter Selection	
SW1 Position	Digital Input
-1	IN0 / INT
-2	IN1
-3	IN2
-4	IN3
-5	IN4
-6	IN5
-7	IN6
-8	IN7

Host Interrupt

The RELAYIO-104 provides the capability to optionally generate a host interrupt when digital input #0 becomes activated. This feature is particularly useful for counting pulses or when applications must provide immediate attention to important external events.

Host Interrupt Configuration

Jumper block J8 configures which host interrupt will be associated with the RELAYIO-104. Any interrupt may be used but the optional J2/P2 connector is required to access the upper interrupt request channels (IRQ10, 11, 12, 14 or 15). An interrupt is selected by placing a shorting jumper between the center row of J8 and the corresponding interrupt pin. Interrupt capability is disabled by placing a shorting jumper at the DIS position of J8 (factory default). The interrupt driver on the RELAYIO-104 conforms to the method for interrupt sharing as outlined in the PC/104 specification. This method recommends that one of the PC/104 modules sharing an IRQ provide a passive pull-down resistor to ground. The RELAYIO-104 can supply the pull-down resistor when a shorting jumper is installed at the PD position of J8. The pull-down resistor has no effect when interrupts are disabled.

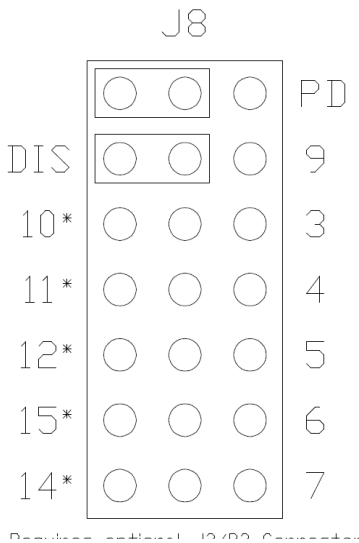


Figure 4 - J8 Interrupts Configuration

Try selecting an interrupt which is not currently being used by other system resources. Certain interrupts have a de-facto standard usage and should be avoided. If interrupts must be shared make sure all the software applications and hardware involved support interrupt sharing. To prevent excessive current draw and the possibility of erroneous operation, use only one pull-down per IRQ. Interrupt #9 is re-directed to IRQ2 on most AT style computers.

INT_STAT - Interrupt Status Register 0x02

The **INT_STAT** (Interrupt Status) register is used to monitor and determine if interrupt requests are being generated by the RELAYIO-104. It is also used to remove an interrupt request after it has been recognized and serviced. Applications which do not need full interrupt capability can simply poll the **INT_STAT** register to see if digital input #0 has become or was previously activated.

Bit	7	6	5	4	3	2	1	0	
(0x02)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**IS**	**INT_STAT**
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

IS **Interrupt Status Bit**

This bit is set whenever digital input #0 changes from a de-activated to an activated state. The event is latched keeping the bit set even if digital input #0 is activated for only a short time. Jumper block J8 must be properly configured for the interrupt request to be passed up to the host. The **IS** bit is cleared by writing any byte value the **INT_STAT** register. It is automatically cleared during system reset.

Interrupt Circuitry and Timing Sequence

The interrupt circuitry functional diagram and timing sequence are shown below. Whenever sufficient voltage and current are applied to digital input #0 it changes from a de-activated to an activated state forcing the output of the opto-isolator to switch to logic "0". This signal is routed to the inverter (via the optional AC filter) which then outputs a logic "1" and clocks the flip-flop on the rising edge. This in turn causes its "Q" output to become logic "1". The state is echoed in the **IS** bit in the Interrupt Status Register and simultaneously enables the tri-state interrupt driver. If the input signal is actually a momentary pulse the event is stored by virtue of the flip-flop. If interrupts are properly configured the driver then sends an interrupt request to the host as determined by the J8 jumper settings. The request invokes an interrupt service routine on the host. If interrupts are shared, the host can first examine the **IS** bit to determine if the RELAYIO-104 is causing the request. The **INT_STAT** register must be written to during the interrupt service routine to reset the flip-flop which in turn clears the **IS** bit and releases the interrupt request.

Digital input #0 is **NOT** Schmitt triggered. When using it for interrupts the driving signal should have clean sharp edges to prevent spurious or multiple interrupts requests.

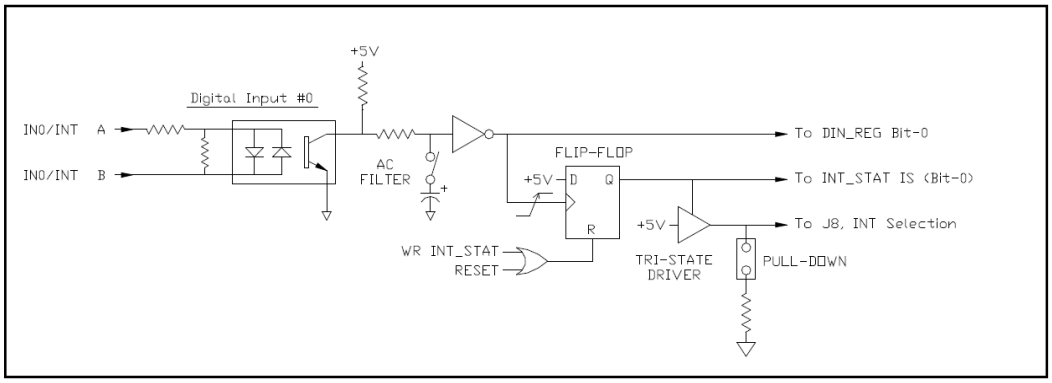


Figure 6 - Interrupts Circuitry Block Diagram

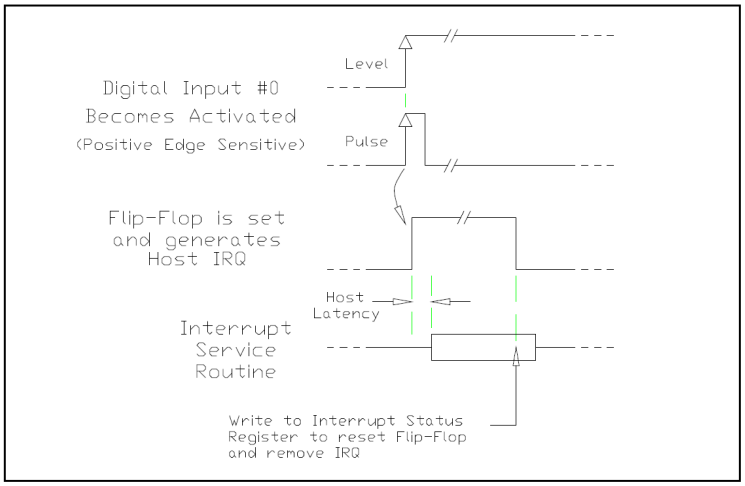


Figure 7 - Interrupt Timing Sequence

Specifications

General:

Description:	PC/104 peripheral board featuring eight relay outputs and eight isolated AC / DC digital inputs
I/O connections:	40 Positions IDC type header
Isolation (All I/O):	250V DC or AC, board-to-field. Isolation between I/O signals: 100V maximum
Power Requirement:	+5Vdc ±5% @ 80ma typical. Additional 30ma required for each activated relay output
Dimensions:	PC/104 compliant, 3.55"W x 3.775"L. 8-bit stack-through, optional 16-bit stack-through with J2/P2 connector
Addressing:	8-bit PC/104 bus. Occupies any consecutive 4-byte block in the host's I/O map, 0x000 through 0x3fc
Environmental:	Operating temperature: -20ºC to 70ºC Non-condensing relative humidity: 5% to 95%
Compliance:	Contains lead / RoHS compliant by exception
Product Origin:	Designed, Engineered, and Assembled in USA by SCIDYNE® Corporation

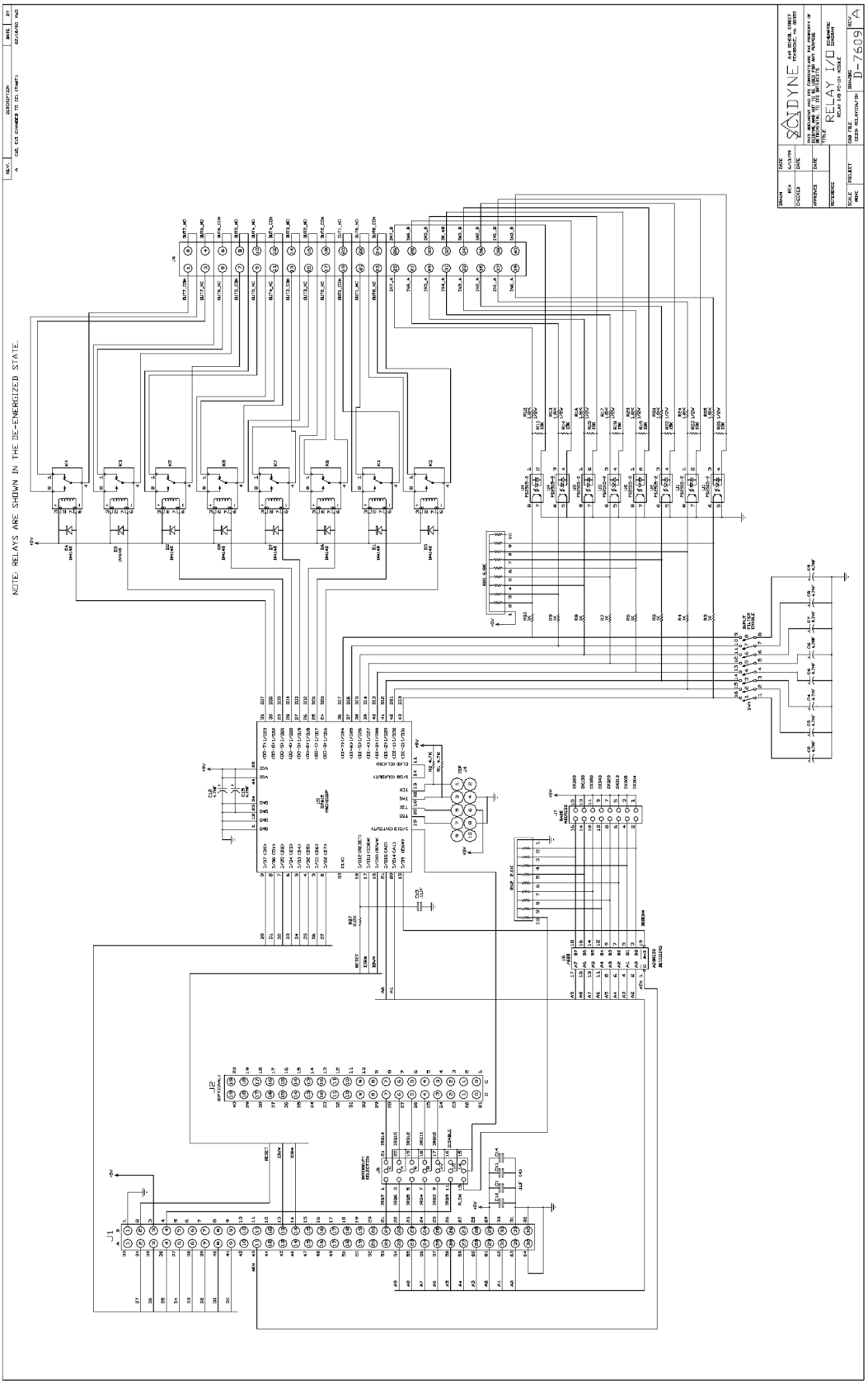
Relay Outputs:

General:	Eight SPDT (Form C) sealed electro-mechanical relays, Break-Before-Make operation
Power Handling:	
DC:	1 Ampere @ 30Vdc maximum
AC:	0.5 Ampere @ $125V_{RMS}$ maximum (resistive load)
Switching capacity:	1ma, 5Vdc minimum, 62.50 VA, 30W maximum
Contact resistance:	100mΩ maximum, Ag (Au clad) contacts
Operate time:	5ms maximum (activate or release)
Service life:	5×10^6 operations minimum

Digital Inputs:

General:	Eight independent non-polarized optically isolated inputs
Input Voltages:	
DC:	3V minimum, 24V maximum, non-polarized
AC:	3VPP minimum, 24VPP maximum, 40hz to 1khz
Switching time:	Typical @ 5V, Filter Disabled: On: 40µs Off: 100µs Filter Enabled: On: 20ms Off: 85ms
Input impedance:	1.8kΩ minimum
AC input filter:	RC type low-pass. Selectable on a per input basis
Interrupt:	One interrupt, Jumper selectable IRQ 3, 4, 5, 6, 7, 9, (10, 11, 12, 14, 15)* or Disable. Fully supports sharing. Associated with digital input #0 activation, positive edge sensitive. * Optional J2/P2 connector required if upper interrupts will be used.

Appendix-A: Schematic Diagram



User Notes