USER'S REFERENCE MANUAL

P8-16

16 Bit Bus Access Adapter for PROTO-8

Model No. 100-7578
Doc. No. M7578 Rev: 1.1 06/22/06

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Previous revision: 1.0 3/11/98

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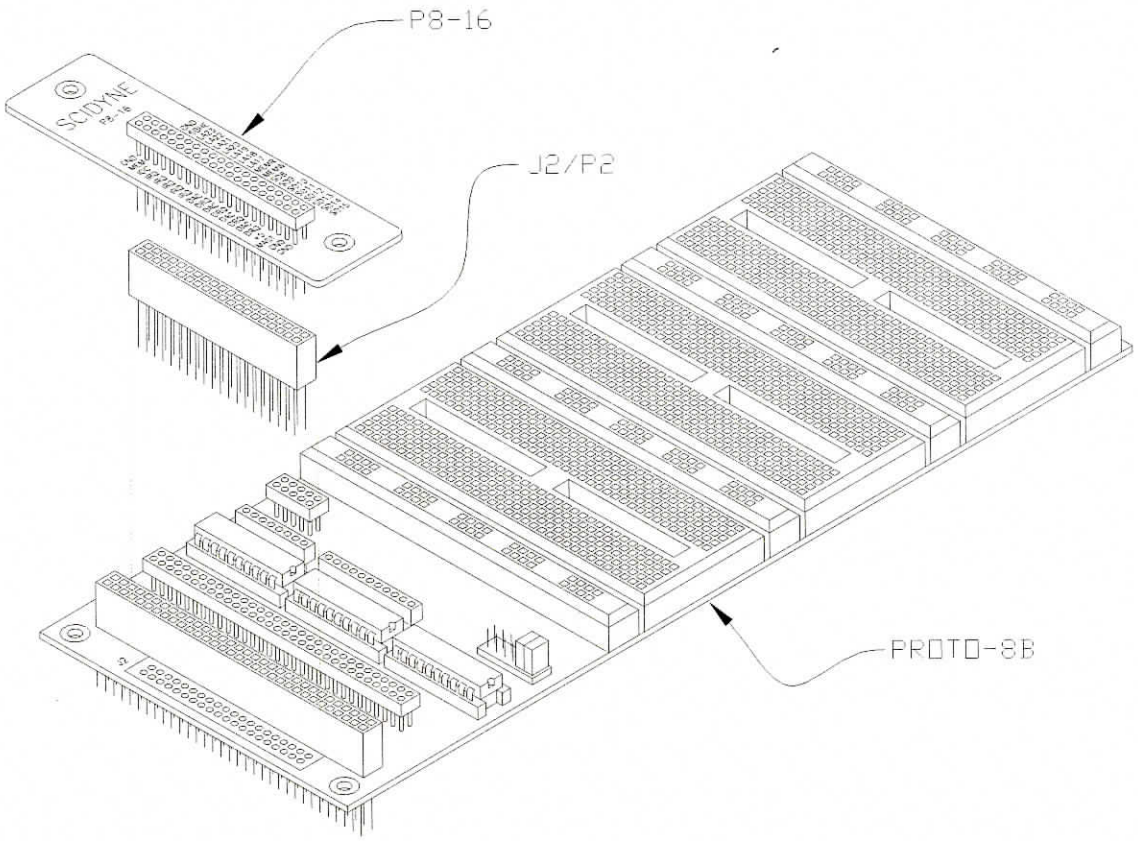
Introduction

The P8-16 is a companion product for use with our PROTO-8 PC/104 prototyping breadboard. The adapter provides simple and cost effective means to upgrade a standard PROTO-8 for use in 16 bit projects. This allows a user to rapidly evaluate and develop more advanced PC/104 designs. The P8-16 simply plugs into the J2/P2 connector located on the PROTO-8. All J2/P2 signals are routed to a socket strip which directly accepts 20-28AWG solid wire or component leads. Each signal is clearly identified, reducing the chances of wiring errors and making connections straight forward. All the original functionality of the PROTO-8 is maintained while at the same time providing a clear path to 16 bit hardware development. The P8-16 may be freely unplugged and re-installed as the user switches between 8 and 16 bit projects.

NOTE: *The J2/P2 connector is not installed on a stock PROTO-8. This connector is required to use the P8-16 and must be purchased separately. Order part number 104-0002.*



Signal Descriptions

NOTE: *An in depth explanation for each signal's purpose and its use is beyond the scope of this manual. Many excellent books exist which fully describe the operation of the PC/104 and ISA bus architecture. The reader is encouraged to seek one of these for a definitive reference.*

PC/104 J2/P2 Signal Descriptions (Listed Alphabetically)		
Signal Name	I/O	Description
DACKx*	O	**DMA Acknowledge** These lines are used to acknowledge DMA requests (DRQ5 - DRQ7) and to refresh system dynamic memory (DACK0). They are active low. (DACK1* - DACK3* are located on the J1/P1 connector.)
DRQx	I	**DMA Request** These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ7 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). The DRQ line must be held high until the corresponding DACK line goes active (low). (DRQ1 - DRQ3 are located on the J1/P1 connector.)
IOCS16*	I	**Input/Output Chip Select 16** Used by an I/O device to indicate that it supports 16 bit accesses. This signal is ignored during memory access cycles.
IRQx	I	**Interrupt Request** These lines are used to signal the processor that an I/O device requires attention. Lower IRQ numbers have higher priority. An Interrupt Request is generated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the processor (interrupt service routine).
LA17 - LA23	O	**Latchable Address** These system address lines must be latched on the falling edge of BALE if they are required for the entire bus access cycle.
MASTER*	I	**Master (16 Bit)** Used by bus masters to indicate 16 bit data size.
MEMCS16*	O	**Memory Chip Select 16** Used by a memory resource to indicate that it supports 16 bit accesses. This signal is ignored by refresh and DMA controllers during I/O cycles.
MEMR* MEMW*	O	**Memory Read** This command line instructs a memory device to drive its data on to the data bus. It performs the same function as SMEMR* except that MEMR* can signal a read operation beyond the first one megabyte of system memory. It may be driven by the processor or the DMA controller. This signal is active low. **Memory Write** This command line instructs the memory device to store the data present on the data bus. It performs the same function as SMEMW* except that MEMW* can signal a write operation beyond the first one megabyte of system memory. It may be driven by the processor or the DMA controller. This signal is active low.
SBHE*	O	**System Byte High Enable** Driven by the bus master to indicate that valid data resides on the upper data lines SD8 - SD15. When active, this signal can be qualified with SA0 to determine if data is 8 bits (SA0=1) or 16 bits (SA0=0) in size.
SD8 - SD15	I/O	**System Data Bus** SD0 - SD7 are located on the J1/P1 connector. SD0 is the least significant bit and SD15 is the most significant bit. The platform byte swapper circuitry assure that SD8-SD15 are valid whenever SBHE* is active.