USER'S REFERENCE MANUAL

DIO24

24 Bit Digital I/O Module for PC/104

Model No. 100-7543
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Conventions and Terminology Used Throughout This Publication

Safety and Usage Conventions

NOTE: *Contains important information and useful tips that will assist in the understanding and operation of the product.*

CAUTION: *Calls attention to a procedure, practice or condition that could possibly cause personal injury or damage to equipment.*

WARNING: *Calls attention to a procedure, practice or condition that could possibly cause severe bodily injury, death or extensive equipment damage.*

Terminology

Host This is the computer or similar device into which the DIO24 is plugged.

Logic conditions Unless otherwise noted, logic signals are designated as TRUE (Set) and FALSE (Clear). Names with an asterisk (*) postscript are inverted or active low. Unless otherwise noted TRUE is considered logic “1" (+5vdc) and FALSE is logic “0" (0vdc).

Numbering Systems Computerized equipment often requires its numeric data to be represented in different forms depending on the audience and information being conveyed. Decimal numbers are typically used for end-user data entry and display while internally these values are converted and manipulated in native binary. Hexadecimal numbers are often used by programmers as an intermediate level between binary and decimal notations.

Base	Name	Format (MS <---> LS)
2	Binary	1011 1001
10	Decimal	185
16	Hexadecimal	0xB9 or $B9_{16}$

Multi-Byte Word Formats

Unless otherwise specified numbers or registers spanning multiple bytes are stored in “little endian” format. The first address (ADDR+0) will contain the Least Significant Byte (LSB) while the Most Significant Byte (MSB) will reside at the highest address.

ADDR+0	ADDR	ADDR+n
LSB	LS <----> MS	MSB

INTRODUCTION

The DIO24 is a 24 bit (channel), non-isolated, digital input/output module specifically designed to provide the high current drive capability required by many peripheral components. It physically conforms to the PC/104 form factor. The 24 channels are grouped across three 8 bit ports as shown in the block diagram below. Unlike competitive products which use a common 8255 chip, each output of the DIO24 can passively source 2.5ma and actively sink 85ma, sufficient sink current to reliably drive solid state and mechanical relays. Each channel may be individually configured as ether an input or output under software control. This feature eases system design by eliminating the necessity to commit an entire port as being used strictly for input or output operations. The lack of a direction register also prevents the problem of all channels resorting back to high impedance inputs during configuration changes or transients caused by inductive loads. Any single input channel can also be used to interrupt the host when that channel changes state. A unique level-edge interrupt detection circuit assures even short duration pulses are recognized. The use of CMOS circuitry provides low power consumption as well as high noise immunity. External peripheral components attach to the DIO24 by means of a 50 conductor IDC type connector. The pinout of this connector is fully compatible with industry standard solid state relay racks.

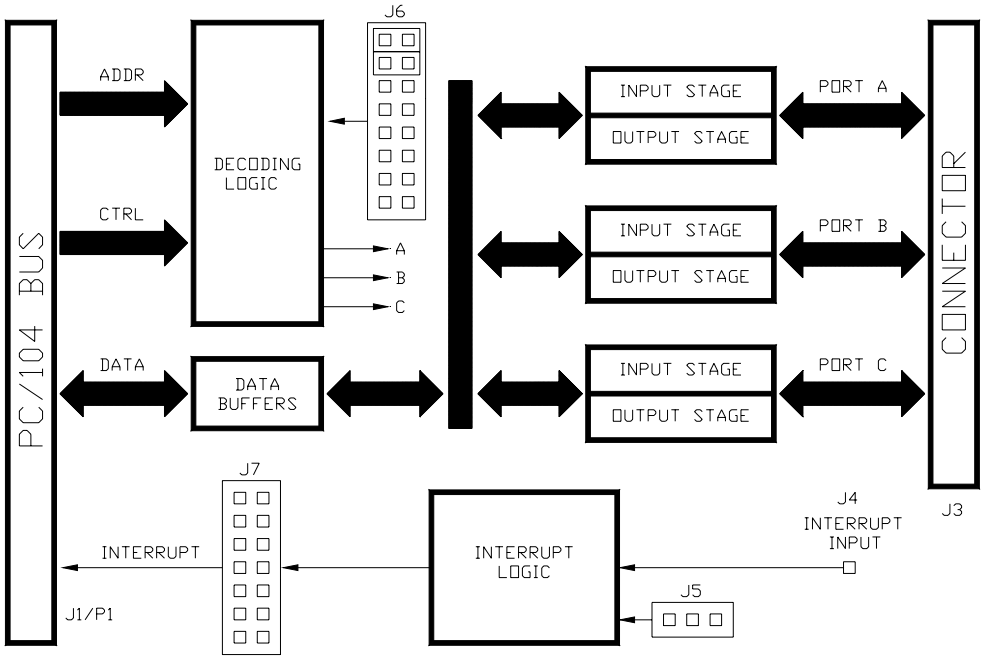

Figure 1 – DIO24 Block Diagram

MODULE SETUP

Before the DIO24 can be put into service it must be properly configured for the desired operating modes. This is accomplished by placing shorting jumpers at various locations on the module. The component identification is shown in figure 2. Each DIO24 comes from the factory set to a basic functional default configuration. The user is free to change the default settings to satisfy any particular application requirements. A full explanation for each of the jumper settings appears on subsequent pages.

DIO24 Factory Default Configuration		
Jumper Block	Function	Default Setting
J4	Interrupt Input Channel Selection	None, No wire jumper installed
J5	Interrupt Edge	J5-A Installed
J6	I/O Base Address	0x300, J6-100 and J6-200 Installed
J7	Host Interrupt	Disabled, No shorting jumpers installed

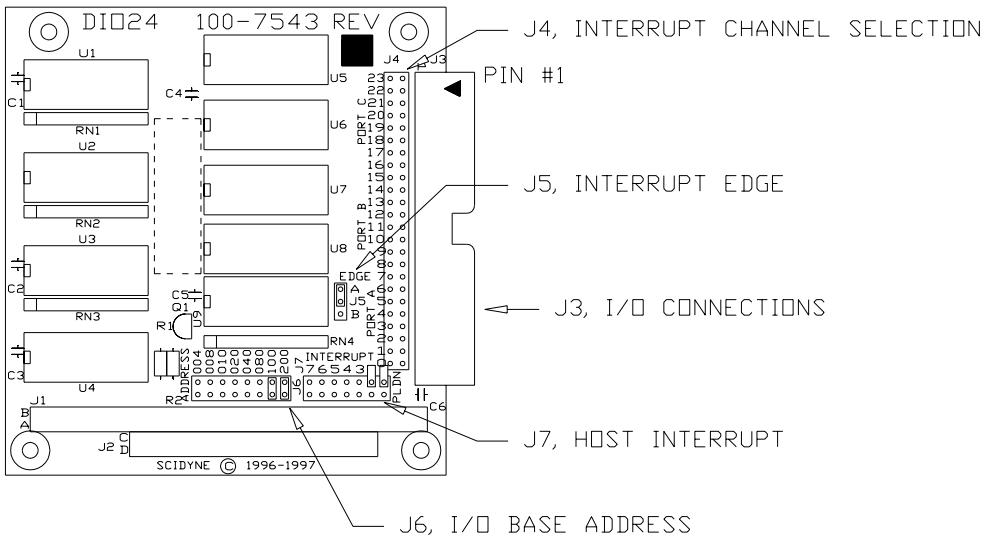

Figure 2 - DIO24 Component Identification

J4 Interrupt Input Channel

The input channel to be used for interrupts is set by soldering a single wire jumper across the appropriate pair of J4 holes. The channel identification numbers (0-23) are clearly printed on the circuit board. If frequent changes to the assignment of the interrupt input channel are anticipated a 24 pin by 2 row jumper block and shorting jumper can be installed instead.

CAUTION: *When installing the wire jumper be sure to use solid wire in the range of 20-24AWG. Follow proper soldering techniques, use only "electronic grade" solder, trim the connections and remove any flux residue remaining on the board.*

SCIDYNE can perform this modification for you when the DIO24 is purchased in production quantities. Contact the SCIDYNE sales department for further details.

J5 Interrupt Edge

The polarity of the input signal which will cause an interrupt is selected by this jumper block. A jumper installed on position J5-A will cause an interrupt when the input changes state from normally high to low. A jumper installed at J5-B will cause an interrupt when the input changes from normally low to high. Some devices, such as solid-state relays, cause an inversion of the signal presented to the DIO24. This in turn transposes the function of jumpers J5-A and J5-B in relation to actual field wiring.

J6 I/O Base Address

The DIO24 occupies four consecutive bytes in the hosts I/O map. The default address of 0x300 can be changed to any four byte boundary in the range of 0x000 to 0x3fc (0 to 1020_{10}). Each position of J6 corresponds to a specific "weighted" address value. The I/O base address is calculated by adding together the "weighted" value for each installed jumper. For example, the factory default address of 0x300 is set by placing shorting jumpers at the 100 and 200 positions while all other locations are left open. The values printed on the circuit board are in hexadecimal notation.

NOTE: *Addresses between 0x000 through 0x0ff are generally used by the host and should be avoided. Make sure the I/O address selected will not conflict with any existing I/O hardware.*

J7 Host Interrupt

Jumper block J7 configures which host interrupt will be associated with the DIO24. The choices are IRQ 9(2), 3, 4, 5, 6 or 7. Interrupt capability is disabled by leaving all positions of jumper block J7 open. The interrupt driver on the DIO24 conforms to the method for interrupt sharing as outlined in the PC/104 specification. This method recommends that one of the PC/104 modules sharing an IRQ provide a passive pull-down resistor to ground. The DIO24 can supply the pull-down resistor when a shorting jumper is installed at the PLDN position of J7.

NOTE: *Try selecting an interrupt which is not currently being used by other system resources. If interrupts must be shared make sure all the software applications involved supports interrupt sharing. To prevent excessive current draw and the possibility of erroneous operation, use only one pull-down per IRQ. IRQ9 is re-directed to IRQ2 on most AT style computers*.

HARDWARE INTERFACE

External devices attach to the DIO24 through J3, a 50 pin IDC type connector. The pinout for J3 is shown below. It is compatible with 8, 16 and 24 position solid state relay racks offered by various manufactures. The DIO24 is also intended to be used to interface switch contacts, relays, LEDs and any other common peripheral devices. A companion terminal board (PN 100-7625/50) is available to make field wiring to these components easier.

J3 Connector Pinout

Bit	PORT A		PORT B		PORT C	
	Base address + 0		Base address + 1		Base address + 2	
	I/O Channel	J3 Pin #	I/O Channel	J3 Pin #	I/O Channel	J3 Pin #
0	CH-0	47	CH-8	31	CH-16	15
1	CH-1	45	CH-9	29	CH-17	13
2	CH-2	43	CH-10	27	CH-18	11
3	CH-3	41	CH-11	25	CH-19	9
4	CH-4	39	CH-12	23	CH-20	7
5	CH-5	37	CH-13	21	CH-21	5
6	CH-6	35	CH-14	19	CH-22	3
7	CH-7	33	CH-15	17	CH-23	1

Special Notes:
1) J3-2 through J3-50 (even pins) are connected to common
2) J3-49 is +5vdc unfused supplied by host

I/O stage operation

Upon system reset the flip/flop's output is cleared deactivating the DMOS transistor and placing it in a high impedance state. The I/O channel is pulled high by virtue of the 2k ohm resistor. Its value has been chosen to supply reasonable source current while the I/O stage functions as an output, yet be capable of being overridden by external devices when used as an input. The level of the I/O channel is presented to the input of the inverting tri-state buffer. Performing an I/O read operation on the corresponding port activates the tri-state buffer and passes the inverted state of the I/O channel to the host computer. As shown, the host computer would read a logic 0 for this bit of the port. If an external device were to pull the I/O channel to common, the computer would then read a logic 1. The users software can perform an invert operation if the actual state of the I/O channel must be represented.

When the I/O stage functions as an output, the 2k pull-up resistor supplies up to 2.5ma of source current to external devices. Performing an I/O write operation to the port with the corresponding I/O channel bit at logic 1 sets the flip/flop which activates the DMOS transistor. The transistor pulls the I/O channel hard to common and provides a low impedance path capable of sinking 85ma. An I/O read operation on this bit essentially returns the logic state stored in the flip/flop due to the double inversion provided by the transistor and buffer. This feature is extremely useful when performing read-modify-write bit manipulations in software on a single channel.

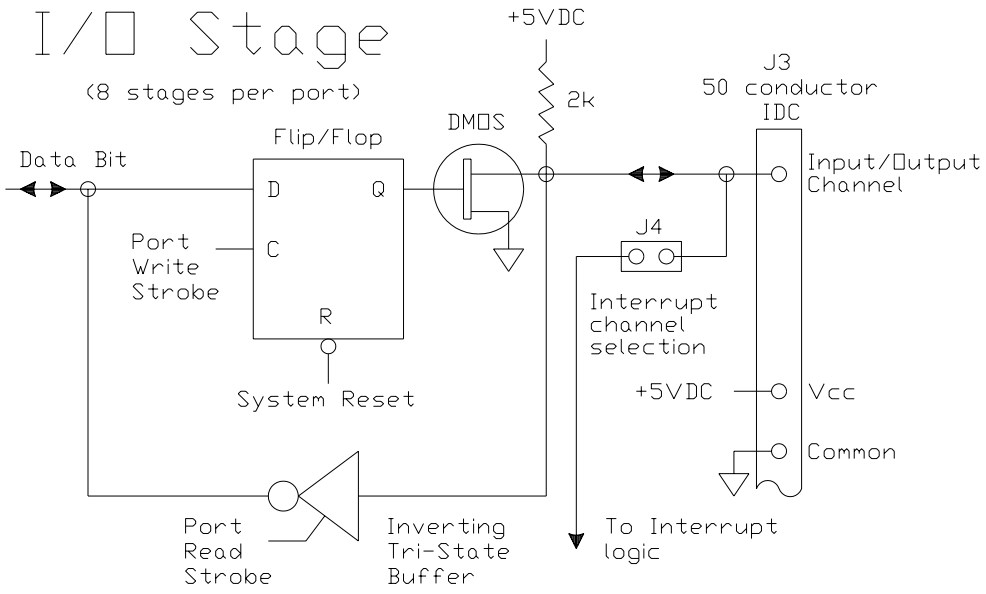

Figure 3 – I/O Stage Circuitry

INTERRUPTS

The DIO24 allows any single channel used as an input to optionally interrupt the host when that channel changes to a predetermined state. Interrupts are detected using a unique Level-Edge circuit. This feature allows external signals to interrupt the host while that signals remains in a predetermined state. It also captures narrow state change transitions which could otherwise be missed using level type interrupts alone. The polarity of the interrupt as well as which host interrupt will be used can be set to suit the users needs. Refer to the module setup section of this manual for further details.

Interrupt Status Register

The Interrupt Status Register is used to monitor interrupts generated by the DIO24. It is also used to clear an interrupt request after it has been serviced by writing any single byte value to it. The IS bit is automatically cleared whenever a system hardware reset occurs.

Interrupt Status Register

B7	B6	B5	B4	B3	B2	B1	B0	
U	U	U	U	U	U	U	IS	Base Address + 3
-	-	-	-	-	-	-	0	Reset

U Undefined

IS Interrupt Status
0 = DIO24 is not requesting interrupt service
1 = DIO24 is requesting interrupt service

Interrupt Timing Sequence

The typical interrupt timing sequence is shown in figure 4. An input normally idles ether high or low as determined by the EDGE setting, jumper block J5. When that input changes state it generates an interrupt request to the host and sets the IS bit in the Interrupt Status Register. If the input signal is actually a momentary pulse the event is stored by the DIO24 Level-Edge circuitry. The request invokes an interrupt service routine on the host. If interrupts are shared, the IS bit can be examined to determine if the DIO24 has caused the request. During the interrupt service routine the input is returned to its idle state by removing the source of the interrupt. This is followed by writing to the Interrupt Status Register which clears the IS bit and releases the interrupt request.

NOTE: *The width of an input pulse must be shorter than the entire duration of the interrupt service otherwise multiple interrupts will occur.*

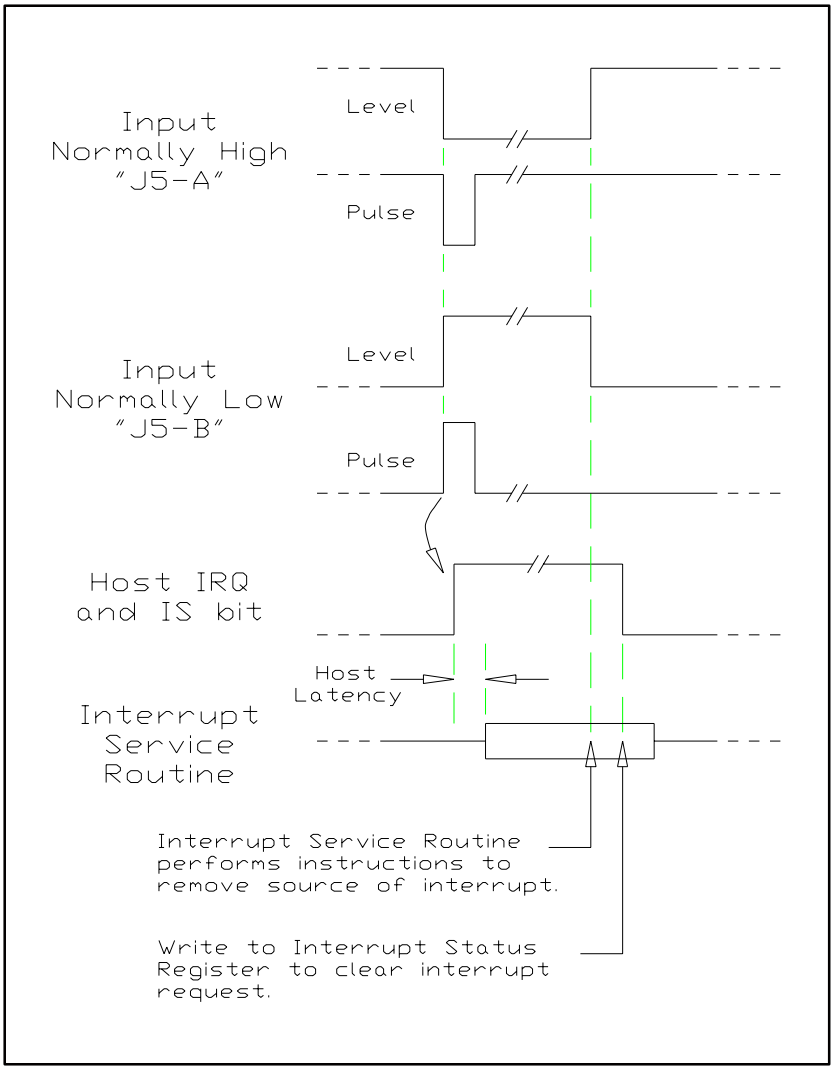

Figure 4 – Interrupt Timing Sequence

SPECIFICATIONS

Number of channels: 24 Individually programmable digital Input/Output channels, non-isolated.

Input level: Logic 0 = 0.8vdc maximum, -0.6vdc minimum
Logic 1 = 2.0vdc minimum, 5.6vdc maximum

Output level: Logic 0 = < 0.4vdc (15ma load)
Logic 1 = > 2.0vdc (1ma load)

Max output current: Per channel Source: 2.5ma
Sink: 85ma

Addressing: 4 consecutive I/O bytes Jumper selectable between 0 and 1020 decimal (0 to 0x3fc hexadecimal)

Interrupt: Any single input channel can be configured to interrupt the host computer when that channel changes state.
Interrupts: IRQ 3, 4, 5, 6, 7, 9 (Note: IRQ9 is re-directed as IRQ2 on most AT computers)
Polarity: Selectable positive or negative level-edge
Pulse detection: 2µs pulse width minimum
Interrupt sharing: Fully supported including interrupt status register

Power requirement: +5vdc ±5% @ 20ma typical, external loads excluded

Dimensions: PC/104 compliant, 3.6"W x 3.8"L. 8-Bit stack-through.
Holes provided for adding J2/P2 connector creating 16-bit stack-through compatibility

Environmental: Operating temperature: -40°C to 85°C
Non-condensing relative humidity: 5% to 95%