PC/104-*Plus* Specification

Version 1.2

August 2001

Please Note

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REVISION HISTORY

Draft 0.7, November 20, 1996 - Preliminary Draft
a. Formatted to meet the requirements of the PC/104 Consortium.
b. Modify the component restrictions across and to each side of the PC/104 connectors (three sides, .400“ from each edge, 4.35" top clearance, .100" bottom clearance).

Draft 0.8, December 16, 1996 - Cleanup for Release
a. Correct general typos.
b. Correct word reference error.
c. Add QuickSwitch part number and clarify Mux requirements.
d. Change PCI ONLY to PCI-Only and add note.
e. Correct figure 4 and Figure 5 errors.
f. Correct typo in Table 3.

Draft 0.9, January 10, 1997 - Cleanup for Release
a. Cleanup minor grammatical errors.

Version 1.0, February 1997 - Initial Release
a. Grammatical changes and cleanup per review recommendations.
b. Change Footnote 1 on Page 2 to show future support for the M66EN (66MHz Enable) signal.
c. Add signals PRSNT[1:2]* and CLKRUN* to Figure 1 to encompass all unused PCI signals.
d. Moved the Mechanical section after the Electrical section.
e. Clarified the KEY pin usage for universal modules and defined them as ground connections.
f. Clarified pin 1 for the PC/104-*Plus* connectors on Figure 4.
g. Added an example manufacturer and part No. for the PCI connector (Figure 5) and Shroud (Figure 6).
h. Modified Figure 2, Table 1, and some text under Section 2.2 to add routing recommendations for the PCI interrupt lines INTA - INTD.

Version 1.1, June 1997 - Minor Editorial Corrections
a. Correct errors in the Table of Figures and Table of Tables.
b. Correct dimensions on the PCI connector (Figure 5).
c. Correct part number and dimensions on the shroud (Figure 6).
d. Correct general typos and update reference information.

Version 1.2, April 2001
a. Added PCI Connector Specifications and PCI-104 name for “PCI Only”.
b. Added PC/104 8-Bit and 16-Bit Connector Specification.
c. Removed specific company references.
d. Corrected PCISIG and consortium addresses and phone numbers.

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1. INTRODUCTION

While the PC/AT architecture is becoming increasingly popular in embedded applications, there is an increasing need for a higher performance Bus throughput. This is especially true when it comes to graphics devices as well as other high speed I/O devices such as networks.

This document supplies the mechanical and electrical specifications for the "PC/104-*Plus*" and incorporates all of the PC/104 features, with the added advantage of the high speed PCI bus. The physical size, mounting configuration and electrical interconnect portion of the PC/104 specification shall remain unchanged.

1.1 Summary of Key Differences From PC/104 Specification:

- A third connector opposite the PC/104 connectors supports the PCI bus.
- Changes to the component height requirements increase the flexibility of the module.
- Control logic added to handle the requirements for the high speed bus.

1.2 Summary of Key Differences (120-pin PCI and PCI Local Bus Specification)

- The PCI bus connector is a 4x30 (120-pin) 2mm pitch stackthrough connector as opposed to the 124-pin edge connector on standard 32-bit PCI Local Bus.
- The 120-pin PCI does not support 64-bit Extensions, JTAG, PRSNT, or CLKRUN signals.

1.3 References

This document covers the addition of the PCI functions. The following documents should be used as reference for a detailed understanding of the overall system requirements:

- PC/104 Specification -- Version 2.4
- PCI Local Bus Specification -- Revision 2.1

Contact the PCI Special Interest Group office for the latest revision of the PCI specification:

PCI Special Interest Group
5440 SW Westgate Drive, Suite 217
Portland, OR 97221
800.433.5177 (U.S.) 503.291.2569 (International)

If errors are found in this document, please send a written copy of the suggested corrections to:

PC/104 Embedded Consortium
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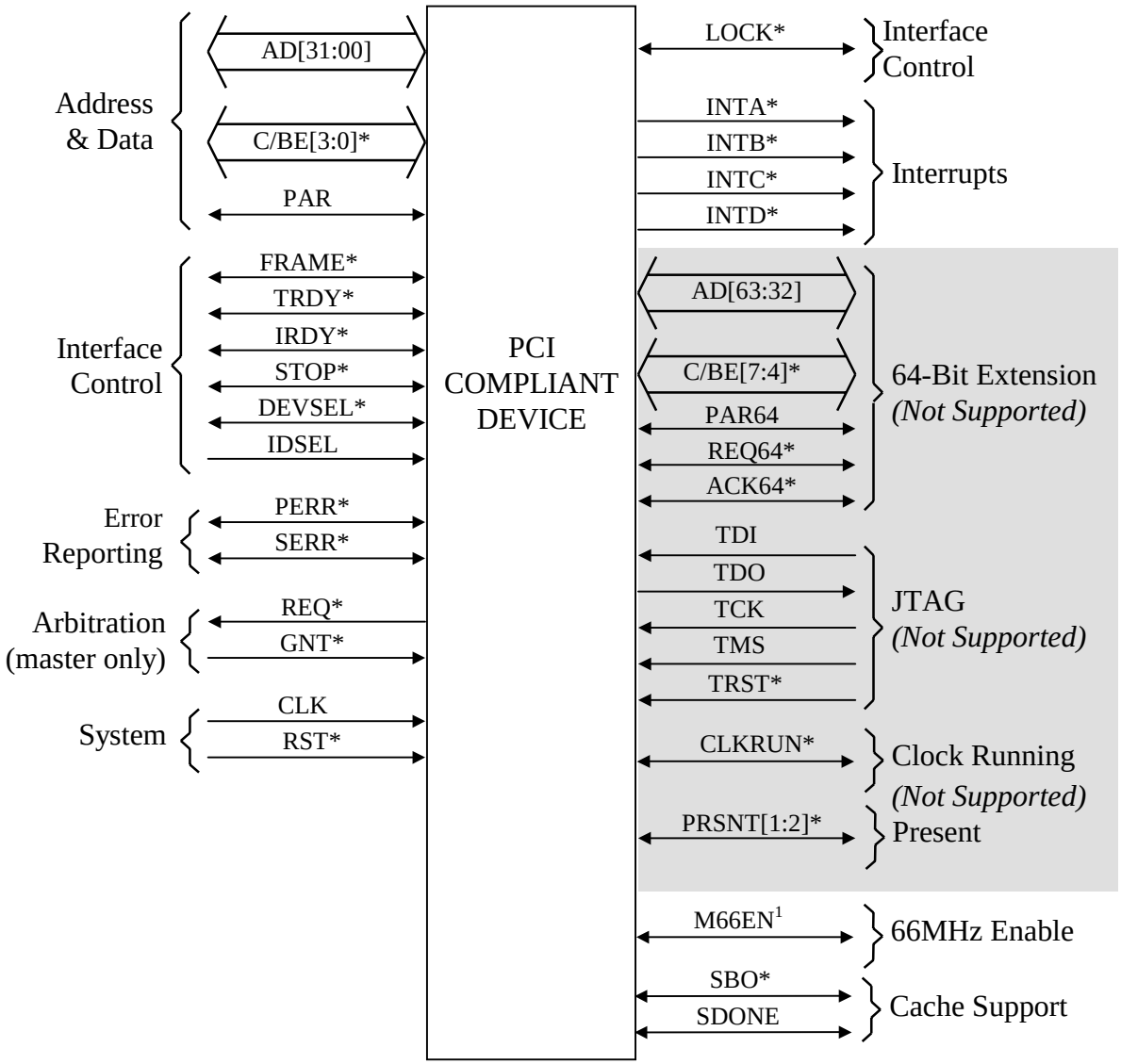
2. PCI SIGNAL DEFINITION

Figure 1 shows the pins in functional groups, with the required pins on the left and the optional pins on the right side. The shaded pins on the right are unsupported features, but are included to show the entire PCI bus as defined in the PCI Revision 2.1 Specification. This version of the PCI bus is intended as a 32-bit bus running at 33MHz and therefore, 64-bit extension and 66MHz[1] are not supported at this time. Also not supported are the boundary scan features (JTAG), *Present* (PRSNR[1:2]*), and *Clock running* (CLKRUN*). The direction indication on the pins assumes a combination master/target device.

Figure 1: PCI Pin List



[1] The PCI bus has been simulated at 33MHz. For the purpose of this specification, 66MHz is not supported. To support future enhancements, the M66EN signal should be grounded on any module that cannot support 66MHz and left open for modules that can support a 66MHz clock.

2.1 PCI Bus Signal Description

2.1.1 Address and Data

AD[31:00]	**Address and Data** are multiplexed. A bus transaction consists of an address cycle followed by one or more data cycles.
C/BE[3:0]*	**Bus Command/Byte Enables** are multiplexed. During the address cycle, the command is defined. During the Data cycle, they define the byte enables.
PAR	**Parity** is even on AD[31:00] and C/BE[3:0]* and is required.

2.1.2 Interface Control Pins

FRAME*	**Frame** is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle.
TRDY*	**Target Ready** indicates the selected devices ability to complete the current data cycle of the transaction. Both IRDY* and TRDY* must be asserted to terminate a data cycle.
IRDY*	**Initiator Ready** indicates the master's ability to complete the current data cycle of the transaction.
STOP*	**Stop** indicates the current selected device is requesting the master to stop the current transaction.
DEVSEL*	**Device Select** is driven by the target device when its address is decoded.
IDSEL	**Initialization Device Select** is used as a chip-select during configuration.
LOCK*	**Lock** indicates an operation that may require multiple transactions to complete.

2.1.3 Error Reporting

PERR*	**Parity Error** is for reporting data parity errors.
SERR*	**System Error** is for reporting address parity errors.

2.1.4 Arbitration (Bus Masters Only)

REQ*	**Request** indicates to the arbitrator that this device desires use of the bus.
GNT*	**Grant** indicates to the requesting device that access has been granted.

2.1.5 System

CLK	**Clock** provides timing for all transactions on the PCI bus.
RST*	**Reset** is used to bring PCI-specific registers to a known state.

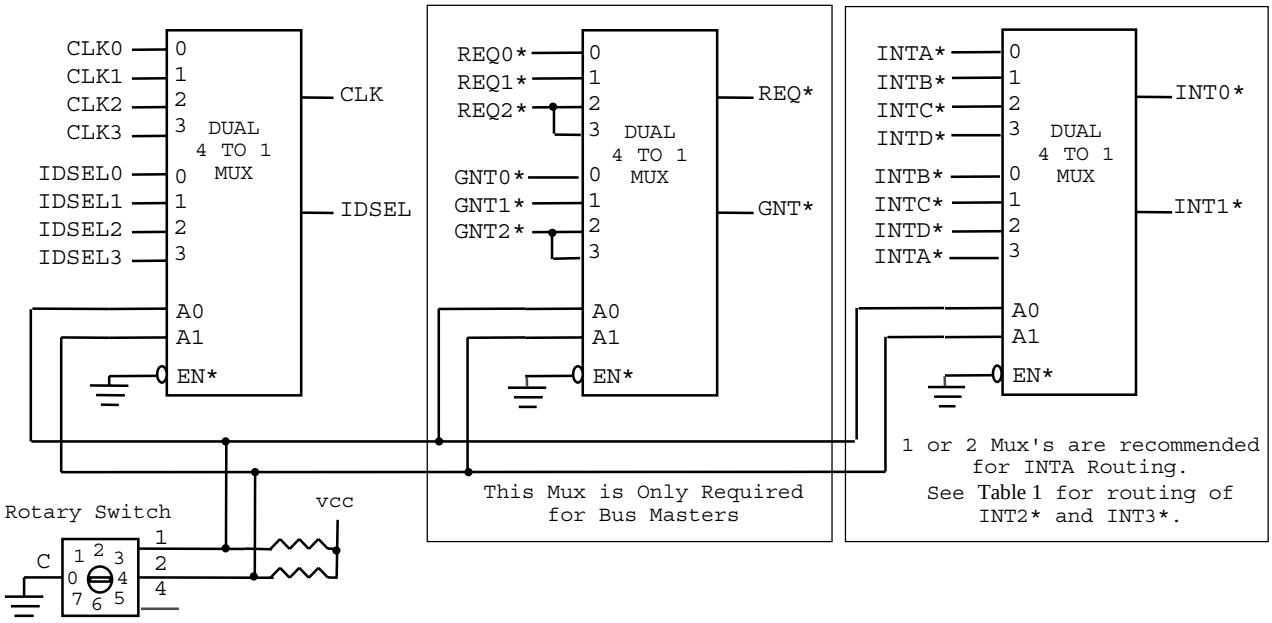
2.1.6 Interrupts

INTA*	**Interrupt A** is used to request Interrupts.
INTB*	**Interrupt B** is used to request Interrupts only for multi-function devices.
INTC*	**Interrupt C** is used to request Interrupts only for multi-function devices.
INTD*	**Interrupt D** is used to request Interrupts only for multi-function devices.

2.2 Signal Grouping

A means of selecting the appropriate signals must be established that will easily allow for the installation and configuration of add-in PC/104-*Plus* modules. Figure 2 shows such a method:

Figure 2: Signal Select



The multiplexer chips are Dual 4:1 Mux/Demux chips. They provide a 5Ω switch that connects the input and output together. These switches provide a bi-directional path with no signal propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. This is typically 250ps at 50pF Load.

Other methods of configuring the modules are possible, but the rotary switch is the most convenient, cleanest and provides for the least possible error in configuration.

The clocks are tuned on the Host Board such that the length of CLK3 trace is ≈0.662" less than CLK2, CLK2 trace is ≈0.662" less than CLK1, and CLK1 trace is ≈0.662" less than CLK0. Therefore, the first module on the stack must select CLK0 (the longest trace), the second CLK1, etc. This provides basically no clock skew between modules. Table 1 shows the appropriate switch setting and signals used for each module in the stack. It is recommended that additional Mux chips be added to route Interrupts if required. Use one Mux for 1 to 2 Interrupts or two Mux's for 3 to 4 Interrupts.

Table 1: Rotary Switch Settings

Switch Position	Module Slot	REQ*	GNT*	CLK	ID Address	INT0*	INT1*	INT2*	INT3*
0 or 4	1	REQ0*	GNT0*	CLK0	AD20	INTA*	INTB*	INTC*	INTD*
1 or 5	2	REQ1*	GNT1*	CLK1	AD21	INTB*	INTC*	INTD*	INTA*
2 or 6	3	REQ2*[1]	GNT2*[1]	CLK2	AD22	INTC*	INTD*	INTA*	INTB*
3 or 7	4	REQ2*[1]	GNT2*[1]	CLK3	AD23	INTD*	INTA*	INTB*	INTC*

Note 1: Because module slots 3 and 4 share REQ2/GNT2, they cannot both be bus master devices.

3. ELECTRICAL SPECIFICATION

3.1 PC/104 Bus

The electrical specifications for the PC/104 bus for bus drive current, bus termination, pullup/pulldown resistors, etc. are unchanged and are defined in the PC/104 Specification. The signal assignments for the J1/P1 and J2/P2 connector are given in Appendix B, Table 4: PC/104 Bus (Reference Only).

3.2 PCI Bus

The PCI Bus mechanical interface is a stackable 30x4 header. This interface carries all of the required PCI signals per *PCI Local Bus Specification Version. 2.1*.

3.2.1 Signal Definitions

For full details on the electrical requirements for the PCI bus, reference the *PCI Local Bus Specification Version. 2.1*.

3.2.2 Signal Assignments

Signals are assigned in the same relative order as in the PCI Local Bus Specification, but transformed to the corresponding header connector pins. Because of the stackthrough nature of the bus, slot-specific signals are duplicated for each plug-in module. The system has been designed to accommodate 4 PC/104-*Plus* modules, so multiple sets of the signals have been duplicated to accommodate one signal for each module. These four signal groups include: IDSEL[3:0] - CLK[3:0] - REQ*[2:0] - GNT*[2:0]. Signal assignments for the J3/P3 connector are given in Appendix B, Table 3: PC/104-*Plus* Bus Signal Assignments.

3.2.3 Power and Ground Pins

The total number of power and ground signals remains the same, but the +3.3 V pins have been reduced by two and the ground pins have been increased by two. The change was the result of signal grouping on the bus and has no effect on performance or integrity.

3.2.4 Key Locations

The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. Universal boards which can support either signal levels will have both key pins implemented. Universal boards must therefore be located at the top of the stack. See Appendix B, Table 3: PC/104-*Plus* Bus Signal Assignments.

3.2.5 AC/DC Signal Specifications

All bus timing and signal levels are identical to the *PCI Local Bus Specification Revision 2.1*.

3.3 Module Power Requirements

Table 2 specifies the voltage and maximum power requirements for each PC/104-*Plus* module. It should be noted that although the maximum requirements as specified are the same as the standard PC/104 Specification, care should be used in designing PC/104-*Plus* modules to guarantee the least possible power consumption. A worst case module as specified could use almost 39 Watts of power, which would basically be unacceptable in most systems.

Table 2: Module Power Requirements

Supply	Min. Voltage	Max. Voltage	Max. Current	Max. Power
+3.3V[1]	3.00	3.60	3A	10.8W
+5V	4.75	5.25	2A	10.5W
+12V	11.4	12.6	1A	12.6W
-5V	-5.25	-4.75	0.2A	1.05W
-12V	-12.6	-11.4	0.3A	3.78W

Note 1: Host Boards implementing “5 volt PCI signaling” are not required to supply 3.3 volts to the modules, but must provide a bus and decoupling. If 3.3 volts is required for a module using the “5 volt PCI signaling” method, provisions should be made to provide its own 3.3 volts by means of an onboard regulator or some other input source. Host Boards implementing “3.3 volt PCI signaling” are required to supply 3.3 volts to the modules.

4. LEVELS OF CONFORMANCE

This section provides terminology intended to assist manufacturers and users of PC/104-*Plus* bus-compatible products in defining and specifying conformance with the PC/104-*Plus* Specification.

4.1 PC/104-*Plus* "Compliant"

This refers to "PC/104-*Plus* form-factor" devices that conform to all non-optional aspects of the PC/104-*Plus* Specification, including both *mechanical* and *electrical* specifications.

4.2 PC/104-*Plus* "Bus-compatible"

This refers to devices which are not "PC/104-*Plus* form-factor" (i.e., do not comply with the module dimensions of the PC/104-*Plus* Specification), but provide male or female PC/104-*Plus* bus connectors that meets both the *mechanical* and *electrical* specifications provided for the PC/104-*Plus* bus connectors.

4.3 PCI-104

Because the PC/104-Plus standard encompasses two different buses (i.e. PC/104 104-pin "ISA" bus and 120-pin "PCI" bus), it is possible for PC/104-*Plus* modules to implement only the PCI bus. Such modules shall have the designation "PCI-104". For example: PCI-104 "Compliant" or PCI-104 "Bus-compatible". This option precludes stacking standard PC/104 Modules.

5. MECHANICAL SPECIFICATION

5.1 Module Dimensions

The mechanical dimensions for this module are identical to PC/104 Specification with the exception of the added connector (J3), some modifications to the I/O connector area, and changes to the component height restrictions. The component height on the top side has been reduced from 0.435" to 0.345" and the bottom has been increased from 0.100" to 0.190". The component restrictions across and to each side of the PC/104 connectors (three sides, 0.400" from each edge) remains the same as the PC/104 Specification. The mechanical dimensions and restrictions are given in Appendix A, Figure 4: Module Dimensions.

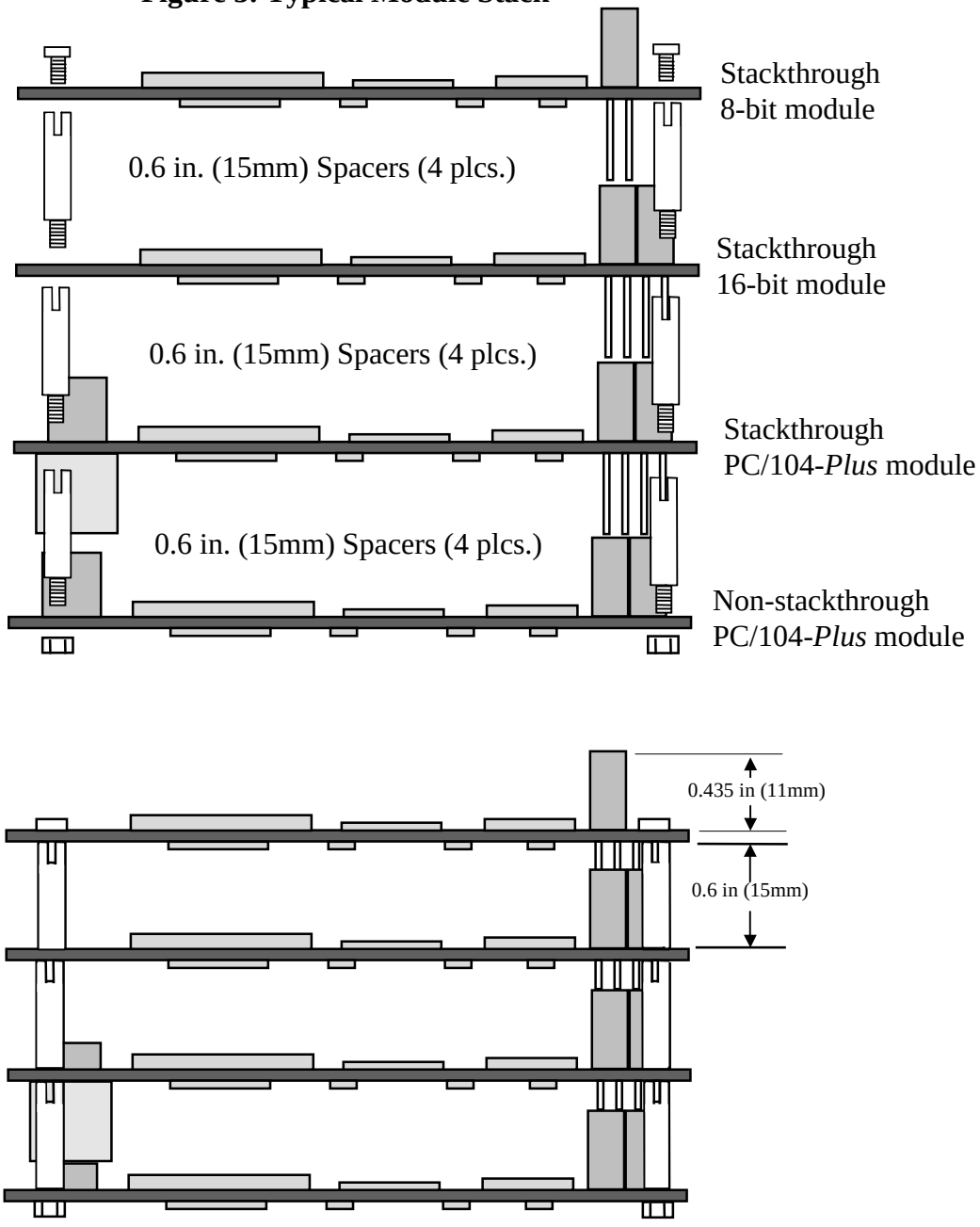
5.2 Connector and Shroud

The PC/104-*Plus* connector for the PCI bus is a 4x30 (120-pin) 2mm pitch connector. The shroud should be installed on the bottom of the PC board when a stackthrough connector is used. The mechanical dimensions and restrictions are given in Appendix A, Figure 5: PC/104-*Plus* and PCI-104 PCI Connector.

6. TYPICAL MODULE STACK

Figure 3 shows a typical module stack with 2 PC/104-*Plus* modules, 1 PC/104 16-Bit module, and 1 PC/104 8-Bit module. The maximum configuration for the PCI bus of PC/104-*Plus* modules is 4 plus the Host Board. If standard PC/104 modules are used in the stack, they must be the top module(s) because they will normally not include the PCI bus.

Figure 3: Typical Module Stack



APPENDIX A

MECHANICAL DIMENSIONS

Figure 4: Module Dimensions

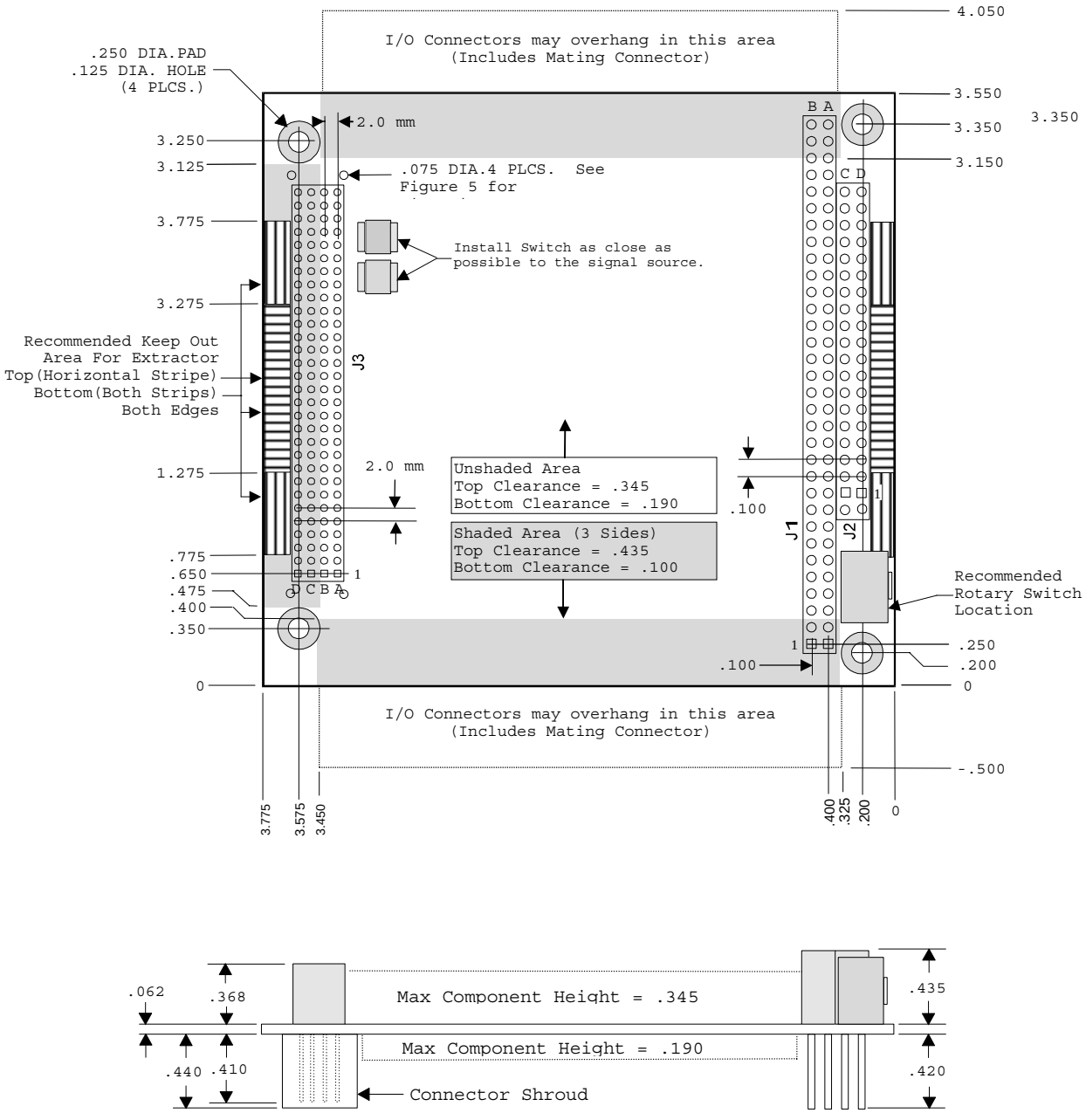


Figure 5: PC/104-*Plus* and PCI-104 PCI Connector

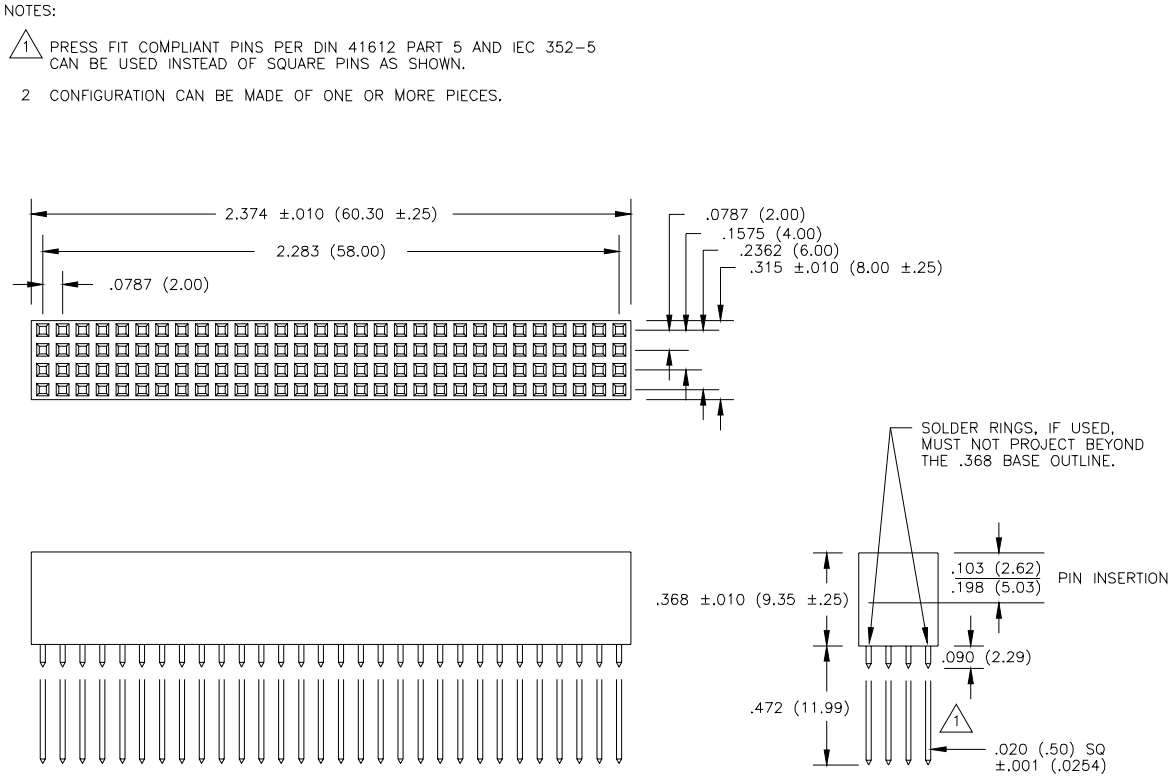


Figure 6: PCI Shroud

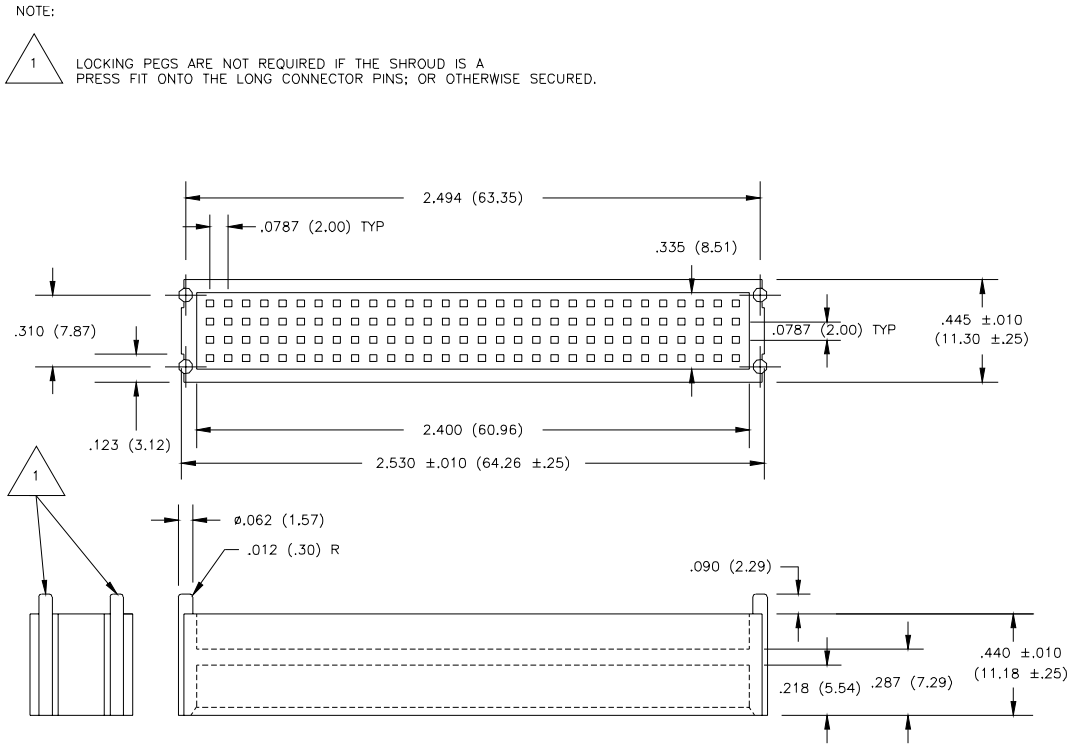


Figure 7: PC/104-*Plus* and PCI-104 PCI Connector Specifications

MATERIALS

HOUSING:	HIGH TEMP THERMOPLASTIC, UL RATED 94-V0
CONTACT:	PHOSPHOR BRONZE
SOLDER:	TIN-LEAD (63-37), IF APPLICABLE
SOLDER CLIP:	ALUMINUM ALLOY, IF APPLICABLE

CONTACT FINISH

FEMALE INTERFACE:	20 MICROINCHES MINIMUM HARD GOLD
MALE INTERFACE:	GOLD FLASH MINIMUM
SOLDER TAIL:	100 MICROINCHES MINIMUM SOLDER
UNDERPLATE:	50 MICROINCHES MINIMUM NICKEL

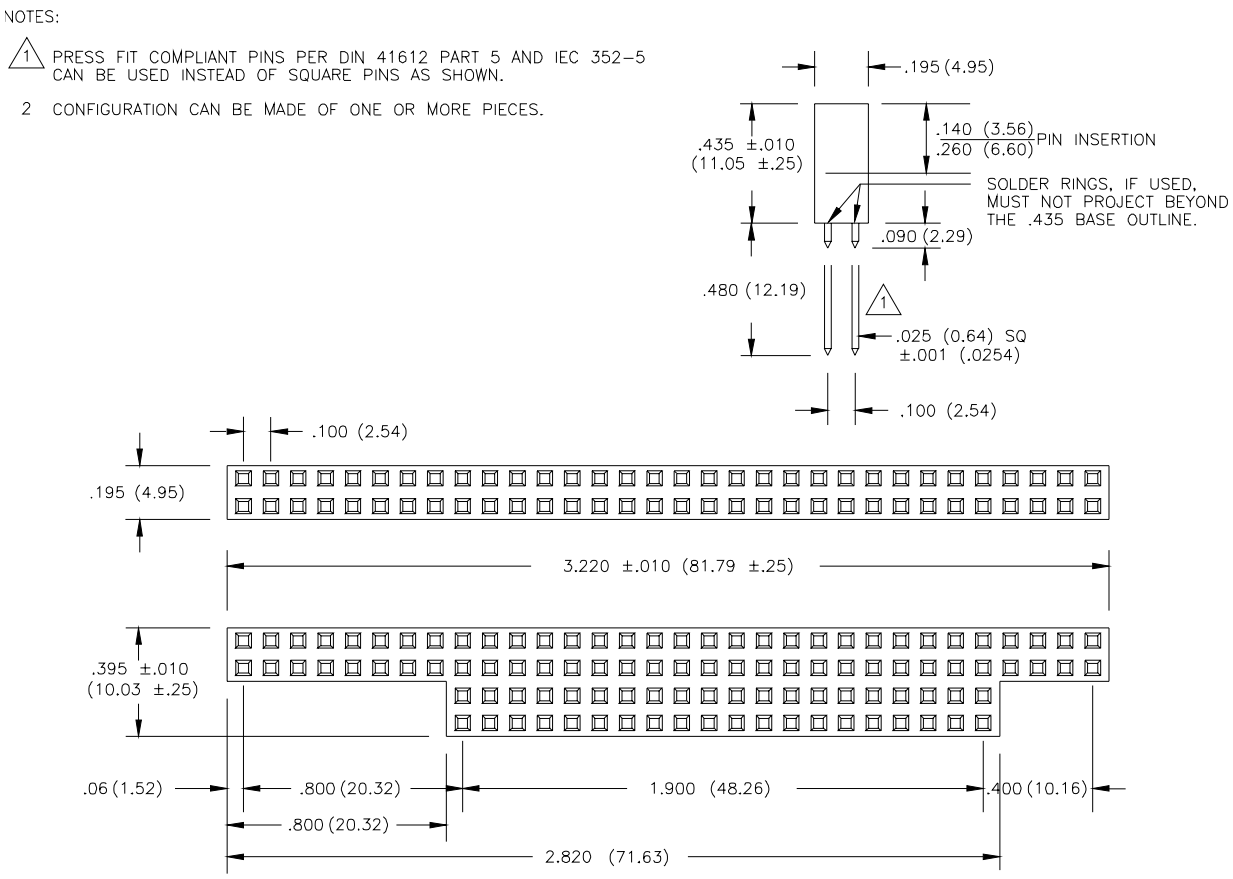
MECHANICAL PERFORMANCE

INSERTION FORCE:	2.5 OUNCE PER PIN MAXIMUM
WITHDRAW FORCE:	1 OUNCE MINIMUM AVERAGE
NORMAL FORCE:	50 GRAMS MINIMUM (PER BEAM)
DURABILITY:	50 CYCLES MINIMUM
OPERATING TEMP:	-55° C TO +85° C

ELECTRICAL PERFORMANCE

CONTACT RESISTANCE:	<30 MILLIOHMS MAXIMUM
CURRENT CAPACITY:	1 AMP CONTINUOUS PER PIN
DIELECTRIC STRENGTH:	500 VAC
INSULATION RESISTANCE:	5,000 MEGOHMS MINIMUM

Figure 8: PC/104 8-Bit and 16-Bit ISA Connector Specification



MATERIALS

HOUSING:	HIGH TEMP THERMOPLASTIC, UL RATED 94-V0
CONTACT:	PHOSPHOR BRONZE
SOLDER:	TIN-LEAD (63-37), IF APPLICABLE
SOLDER CLIP:	ALUMINUM ALLOY, IF APPLICABLE

CONTACT FINISH

FEMALE INTERFACE:	20 MICROINCHES MINIMUM HARD GOLD
MALE INTERFACE:	GOLD FLASH MINIMUM
SOLDER TAIL:	100 MICROINCHES MINIMUM SOLDER
UNDERPLATE:	50 MICROINCHES MINIMUM NICKEL

MECHANICAL PERFORMANCE

INSERTION FORCE:	3.5 OUNCE PER PIN MAXIMUM
WITHDRAW FORCE:	1 OUNCE MINIMUM AVERAGE
NORMAL FORCE:	50 GRAMS MINIMUM (PER BEAM)
DURABILITY:	50 CYCLES MINIMUM
OPERATING TEMP:	-55° C TO +85° C

ELECTRICAL PERFORMANCE

CONTACT RESISTANCE:	<30 MILLIOHMS MAXIMUM
CURRENT CAPACITY:	1 AMP CONTINUOUS PER PIN
DIELECTRIC STRENGTH:	1000 VAC
INSULATION RESISTANCE:	5,000 MEGOHMS MINIMUM

APPENDIX B

BUS SIGNAL ASSIGNMENTS

Table 3: PC/104-*Plus* Bus Signal Assignments

J3/P3				
Pin	**A**	**B**	**C**	**D**
1	GND/5.0V KEY[2]	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY[2]

Notes: 1. The shaded area denotes power or ground signals.

2. The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. It is recommended that both KEY pins (A1 and D30) be electrically connected to GND for shielding.

Table 4: PC/104 Bus (Reference Only)

J2/P2		
Pin	**Row D**	**Row C**
0	GND	GND
1	MEMCS16*	SBHE*
2	IOCS16*	LA23
3	IRQ10	LA22
4	IRQ11	LA21
5	IRQ12	LA20
6	IRQ15	LA19
7	IRQ14	LA18
8	DACK0*	LA17
9	DRQ0	MEMR*
10	DACK5*	MEMW*
11	DRQ5	SD8
12	DACK6*	SD9
13	DRQ6	SD10
14	DACK7*	SD11
15	DRQ7	SD12
16	+5V	SD13
17	MASTER*	SD14
18	GND	SD15
19	GND	KEY

J1/P1		
Pin	**Row A**	**Row B**
1	IOCHCHK*	GND
2	SD7	RESETDRV
3	SD6	+5V
4	SD5	IRQ9
5	SD4	-5V
6	SD3	DRQ2
7	SD2	-12V
8	SD1	ENDXFR*
9	SD0	+12V
10	IOCHRDY	KEY
11	AEN	SMEMW*
12	SA19	SMEMR*
13	SA18	IOW*
14	SA17	IOR*
15	SA16	DACK3*
16	SA15	DRQ3
17	SA14	DACK1*
18	SA13	DRQ1
19	SA12	REFRESH*
20	SA11	SYSCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2*
27	SA4	TC
28	SA3	BALE
29	SA2	+5V
30	SA1	OSC
31	SA0	GND
32	GND	GND